Comparison test case study using Zebax ZX200 vs. WILDER TPA-P Type A HDMI test board

The subsequent pages are test record using Zebax ZX200 HDMI type A test fixture

Test Case : **4Kx2K**
HDMI Clock Frequency: **2.97GHz**

Full comparison chart can be found here:

ZX200-vs-WILDER-4Kx2K-ZXTR-ZX200-AC3-WILDER.pdf

HDMI Compliance Test Software: Measurement Report

Source Tests Report

Configuration

Setup Configuration

Oscilloscope Info	DSA70804 - 5.2.1 Build 8
TDSHT3v1-3 Version	4.0.0 Build 13

Device Configuration

Device Details	HDMI Device
Resolution	4K@297MHz
Refresh Rate	60Hz

Compliance Summary

Total Tests (for all data lanes)	29
Tests Completed	17
Pass	17
Fail	0

Test Summary

Index	Test Name	Lanes	Spec Range	Meas Value	Result
1	7-9 : Source Clock Jitter	CK	Clock Jitter < 0.25*Tbit;	0.099*Tbit	Pass
2	7-10 : Source Eye Diagram	CK - D0	Data Jitter < 0.3*Tbit;	0.13*Tbit	Pass
3	7-10 : Source Eye Diagram	CK - D1	Data Jitter < 0.3*Tbit;	0.13*Tbit	Pass
4	7-10 : Source Eye Diagram	CK - D2	Data Jitter < 0.3*Tbit;	0.14*Tbit	Pass
5	7-6 : Source Inter-Pair Skew	D0 - D1	Skew < 0.2*TPixel;	0.011*TPixel	Pass
6	7-6 : Source Inter-Pair Skew	D1 - D2	Skew < 0.2*TPixel;	0.001*TPixel	Pass
7	7-6 : Source Inter-Pair Skew	D2 - D0	Skew < 0.2*TPixel;	0.01*TPixel	Pass
8	7-4 : Source Rise Time	CK	75.00ps < TRISE;	137.61ps	Pass
9	7-4 : Source Rise Time	D0	75.00ps < TRISE;	124.23ps	Pass
10	7-4 : Source Rise Time	D1	75.00ps < TRISE;	124.05ps	Pass
11	7-4 : Source Rise Time	D2	75.00ps < TRISE;	125.28ps	Pass
12	7-4 : Source Fall Time	CK	75.00ps < TFALL;	137.98ps	Pass
13	7-4 : Source Fall Time	D0	75.00ps < TFALL;	120.50ps	Pass
14	7-4 : Source Fall Time	D1	75.00ps < TFALL;	121.89ps	Pass
15	7-4 : Source Fall Time	D2	75.00ps < TFALL;	122.63ps	Pass
16	7-8 : Max Duty Cycle	CK	Max Duty Cycle < 60.0%;	50.49%	Pass
17	7-8 : Min Duty Cycle	CK	40.0% < Min Duty Cycle;	49.6%	Pass

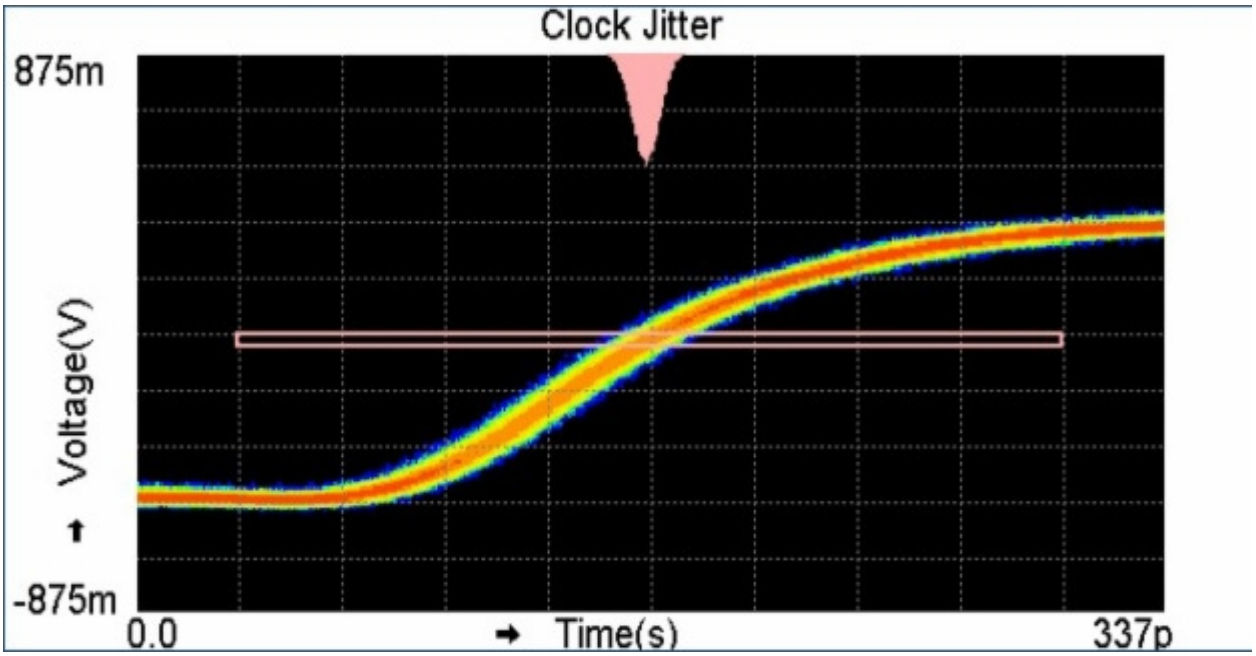
Detailed Results

7-9 : Source Clock Jitter : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Result
Clock Jitter < 0.25*Tbit;	0.099*Tbit	336.71ps	984.20mV	0.15*Tbit	25.000M	Pass

Waveform/Plot



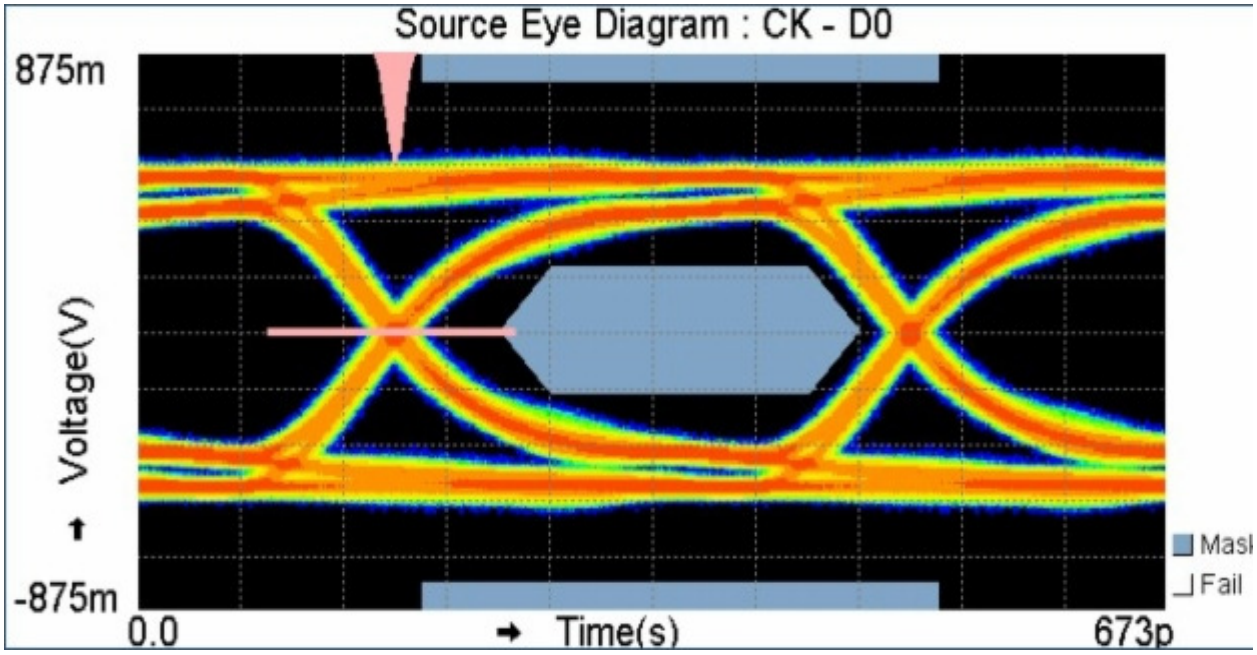
Return to Test Summary

7-10 : Source Eye Diagram : CK - D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask H
Data Jitter < 0.3*Tbit;	0.13*Tbit	336.71ps	962.56mV	174.8m*Tbit	25.000M	0

Waveform/Plot



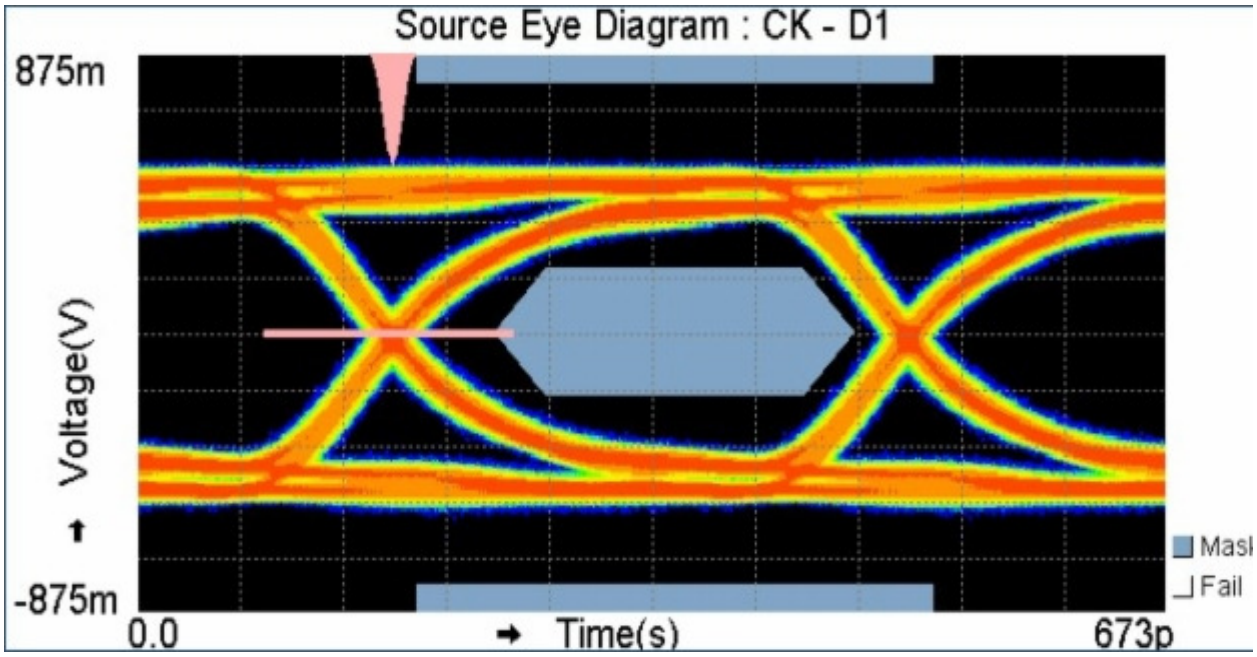
Return to Test Summary

7-10 : Source Eye Diagram : CK - D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask H
Data Jitter < 0.3*Tbit;	0.13*Tbit	336.71ps	950.40mV	169.3m*Tbit	25.000M	0

Waveform/Plot



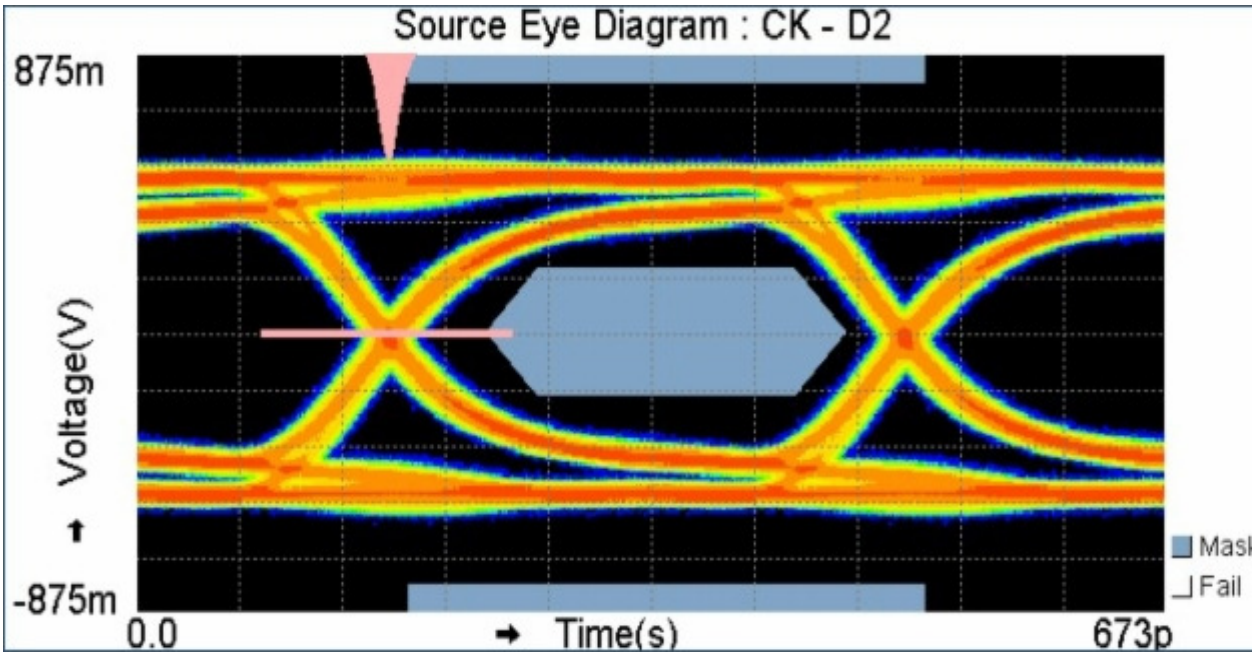
Return to Test Summary

7-10 : Source Eye Diagram : CK - D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Record Length	Mask H
Data Jitter < 0.3*Tbit;	0.14*Tbit	336.71ps	985.12mV	163.3m*Tbit	25.000M	0

Waveform/Plot



Return to Test Summary

7-6 : Source Inter-Pair Skew : D0 - D1

Results

Spec Range	Meas Value	Tbit	Vs(D0 - D1)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.011*TPixel	336.71ps	= 962.56mV, Vs = 950.40mV	33.221p	38.643p	36.044p	Pass

Return to Test Summary

7-6 : Source Inter-Pair Skew : D1 - D2

Results

Spec Range	Meas Value	Tbit	Vs(D1 - D2)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.001*TPixel	336.71ps	= 950.40mV, Vs = 985.12mV	174.88f	5.2703p	2.4866p	Pass

Return to Test Summary

7-6 : Source Inter-Pair Skew : D2 - D0

Results

Spec Range	Meas Value	Tbit	Vs(D2 - D0)	Min	Max	Avg	Result
Skew < 0.2*TPixel;	0.01*TPixel	336.71ps	= 985.12mV, Vs = 962.56mV	30.468p	38.208p	34.224p	Pass

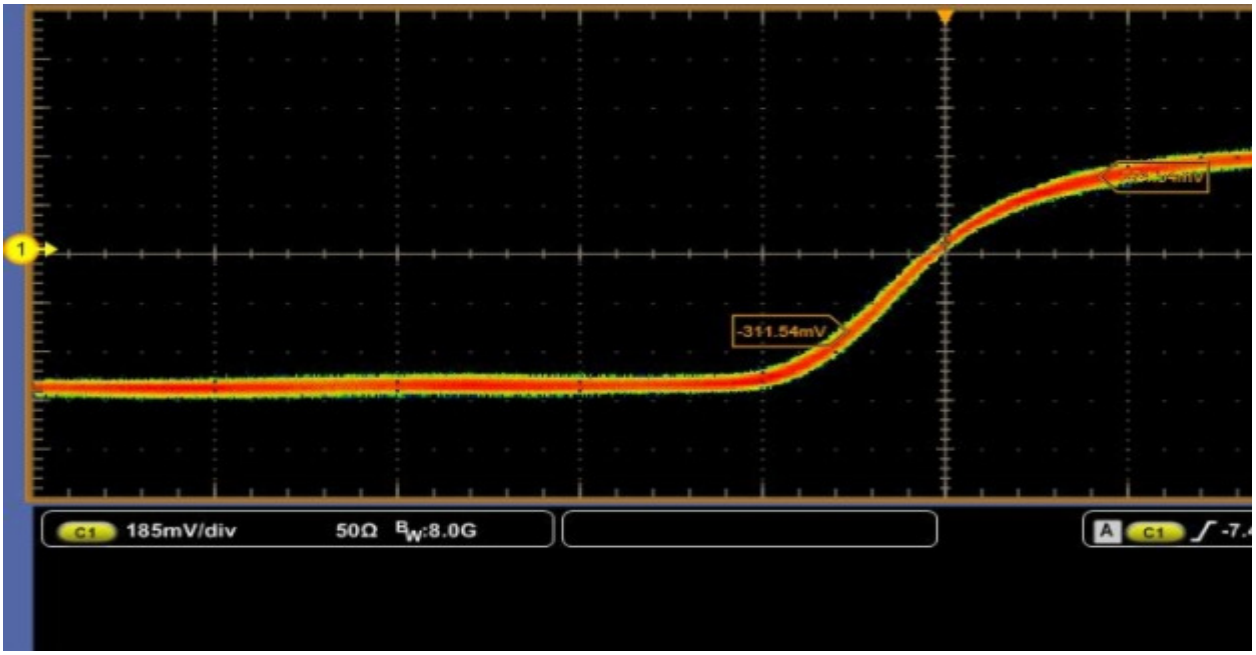
Return to Test Summary

7-4 : Source Rise Time : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	137.61ps	336.71ps	976.80mV	62.61ps	Pass

Waveform/Plot



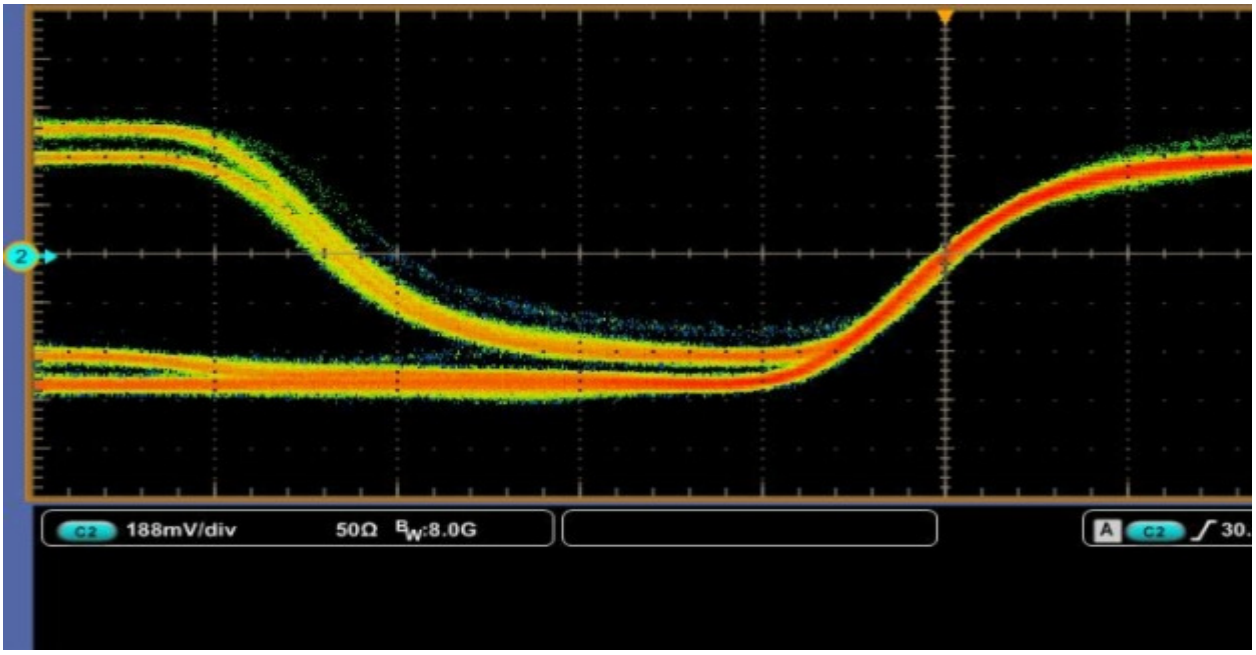
Return to Test Summary

7-4 : Source Rise Time : D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	124.23ps	336.71ps	977.60mV	49.23ps	Pass

Waveform/Plot



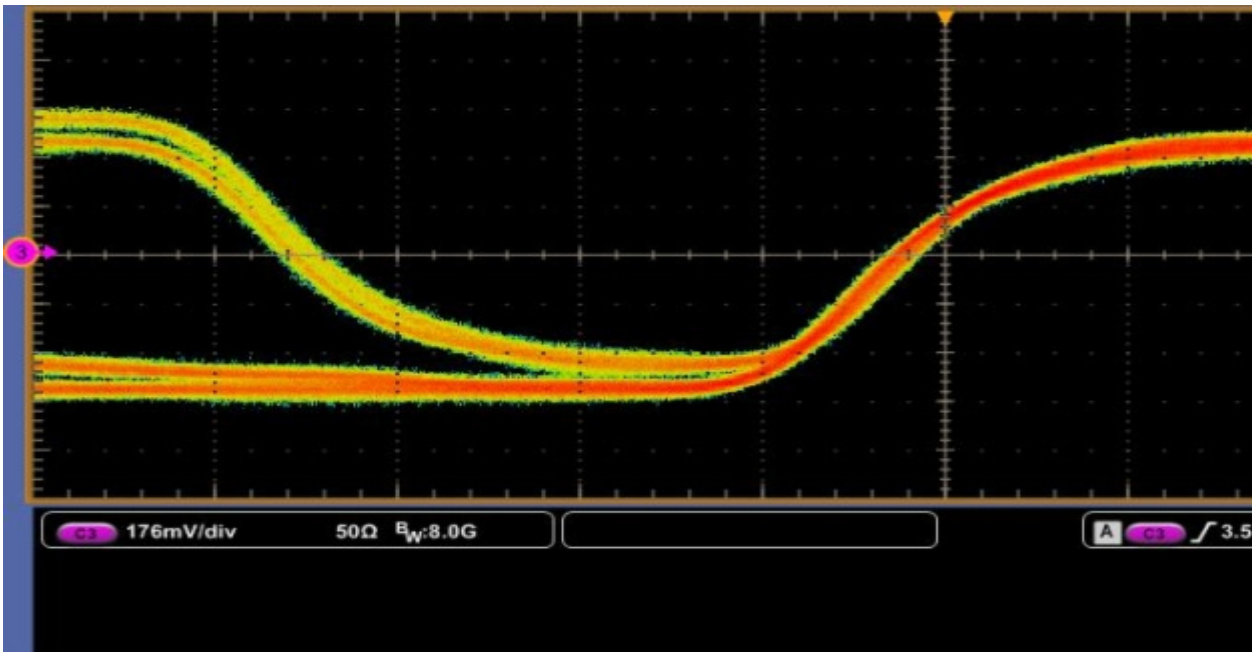
Return to Test Summary

7-4 : Source Rise Time : D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	124.05ps	336.71ps	964.48mV	49.05ps	Pass

Waveform/Plot



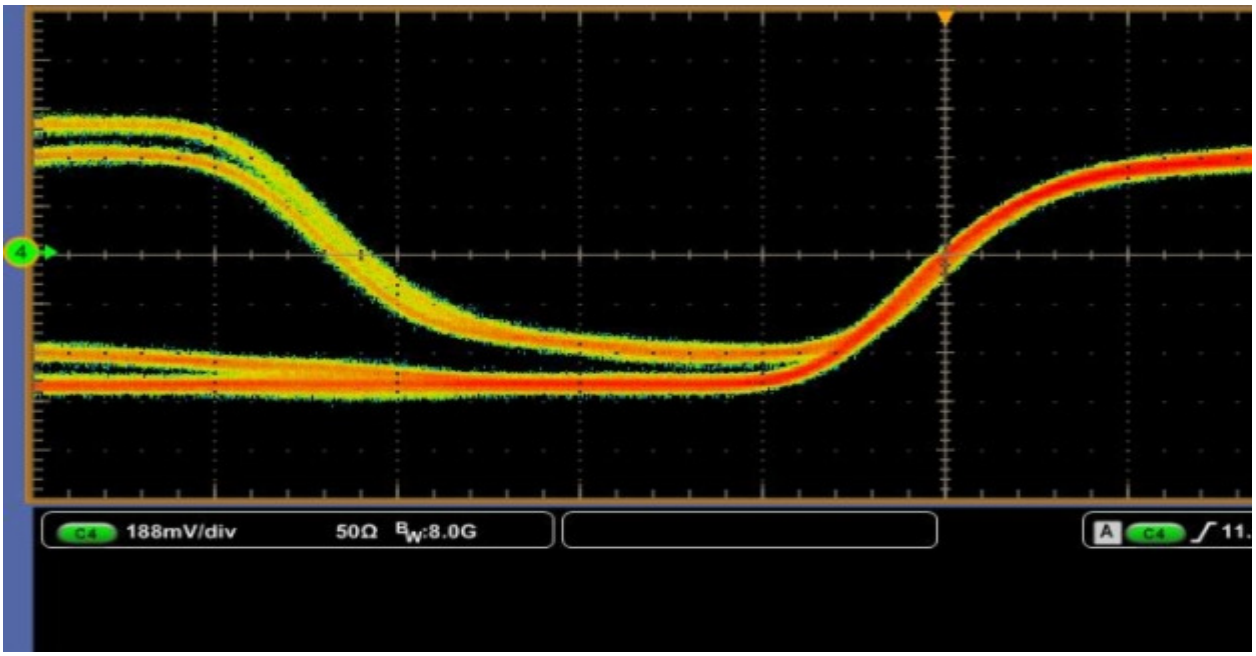
Return to Test Summary

7-4 : Source Rise Time : D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TRISE;	125.28ps	336.71ps	992.64mV	50.28ps	Pass

Waveform/Plot



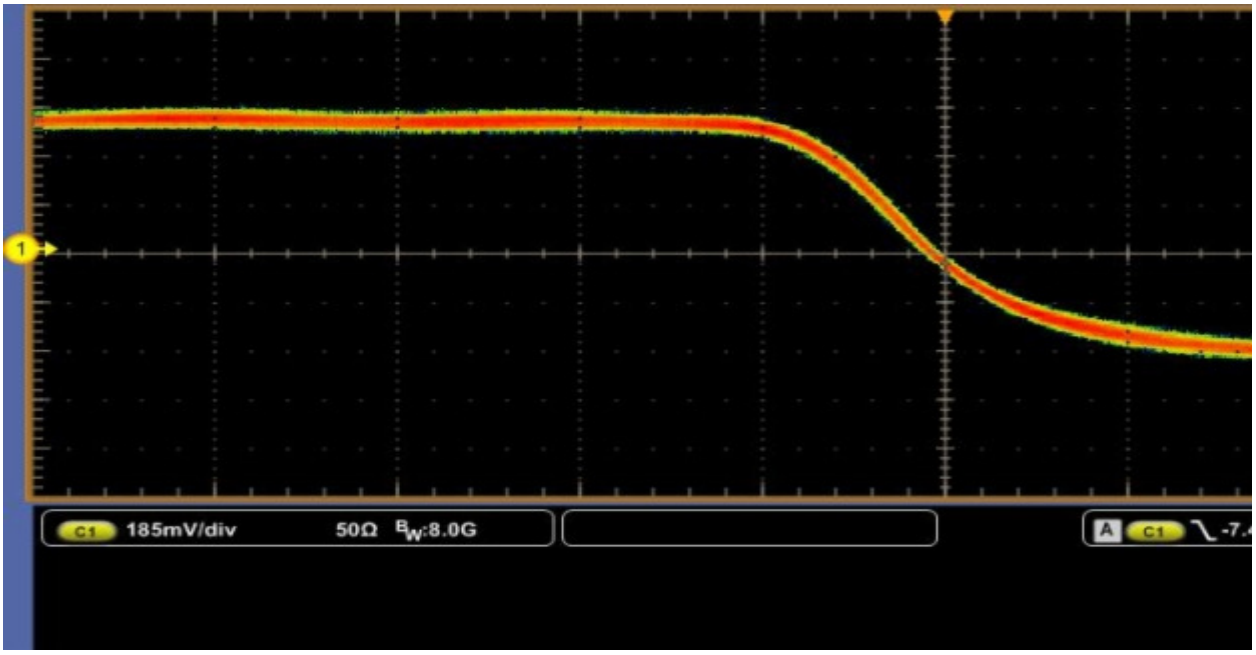
Return to Test Summary

7-4 : Source Fall Time : CK

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	137.98ps	336.71ps	976.80mV	62.98ps	Pass

Waveform/Plot



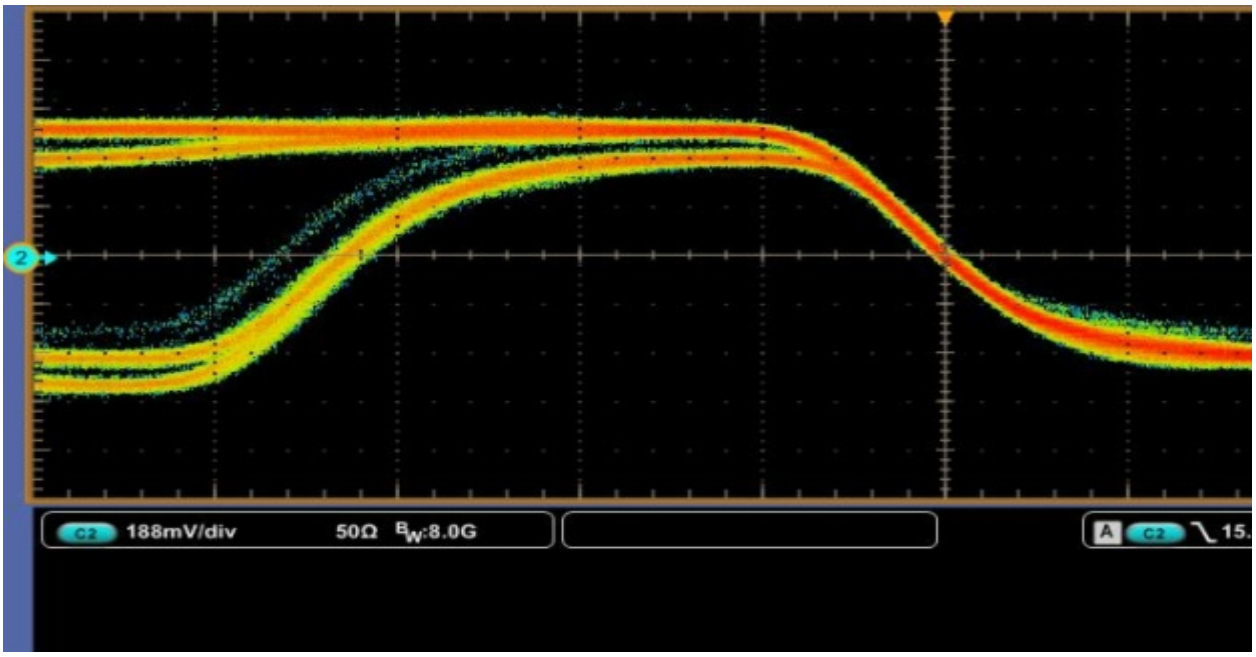
Return to Test Summary

7-4 : Source Fall Time : D0

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	120.50ps	336.71ps	977.60mV	45.50ps	Pass

Waveform/Plot



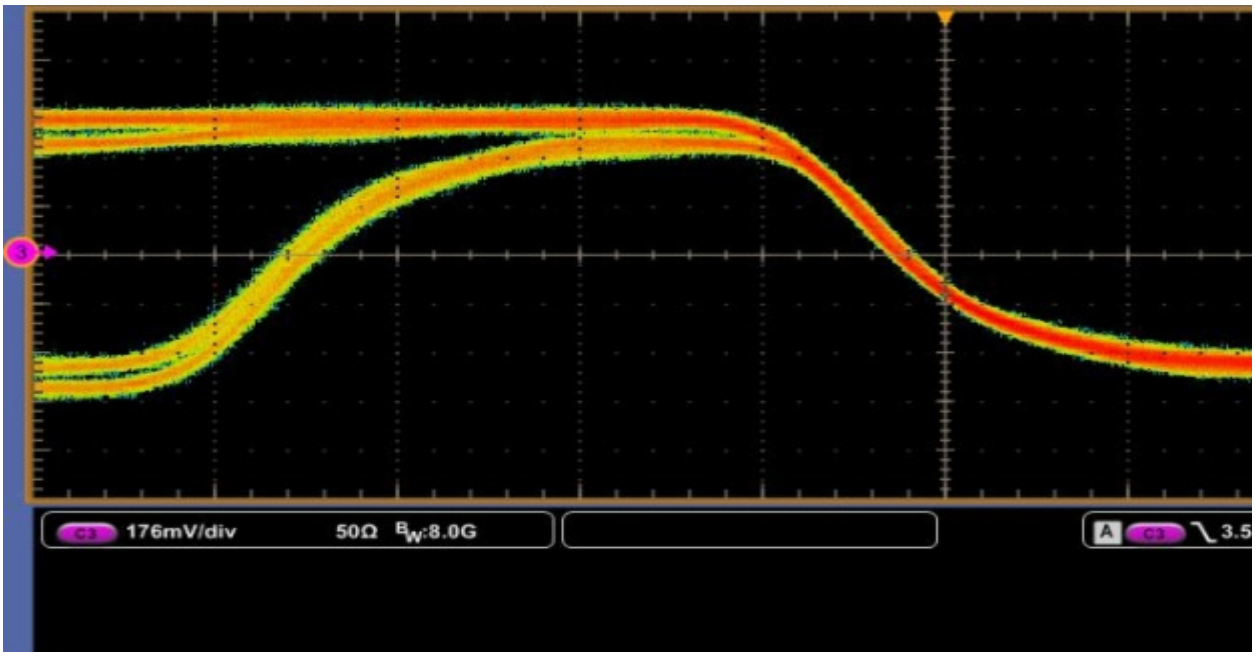
Return to Test Summary

7-4 : Source Fall Time : D1

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	121.89ps	336.71ps	964.48mV	46.89ps	Pass

Waveform/Plot



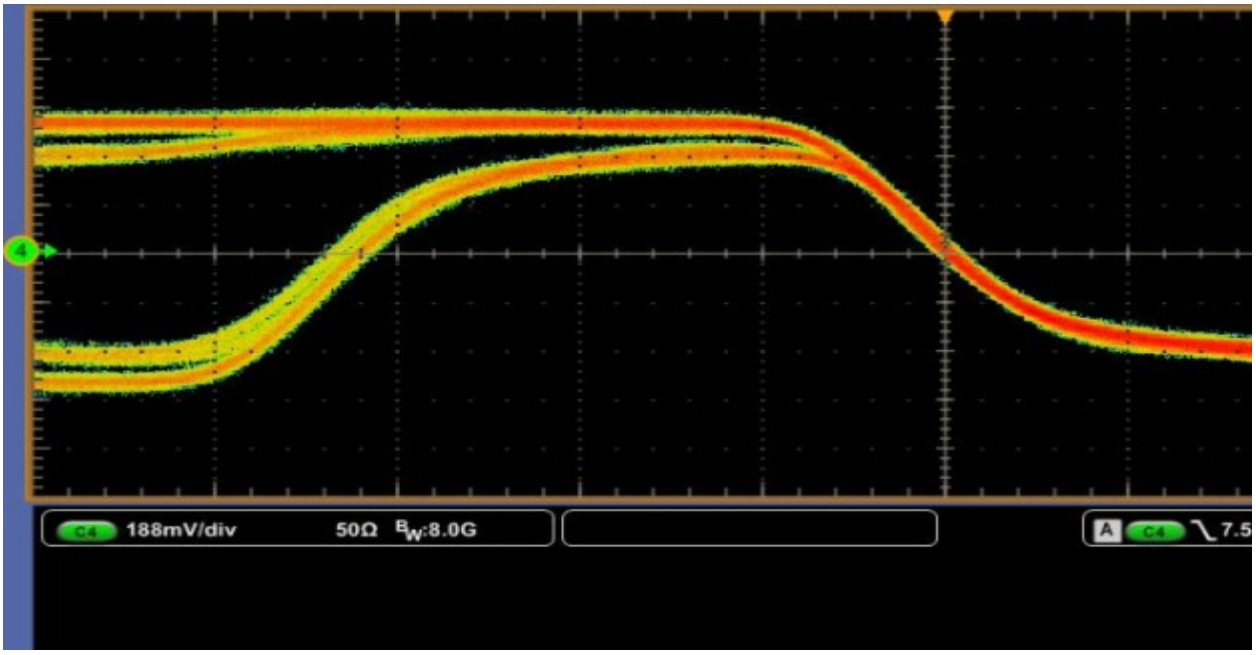
Return to Test Summary

7-4 : Source Fall Time : D2

Results

Spec Range	Meas Value	Tbit	Vs	Margin	Result
75.00ps < TFALL;	122.63ps	336.71ps	992.64mV	47.63ps	Pass

Waveform/Plot



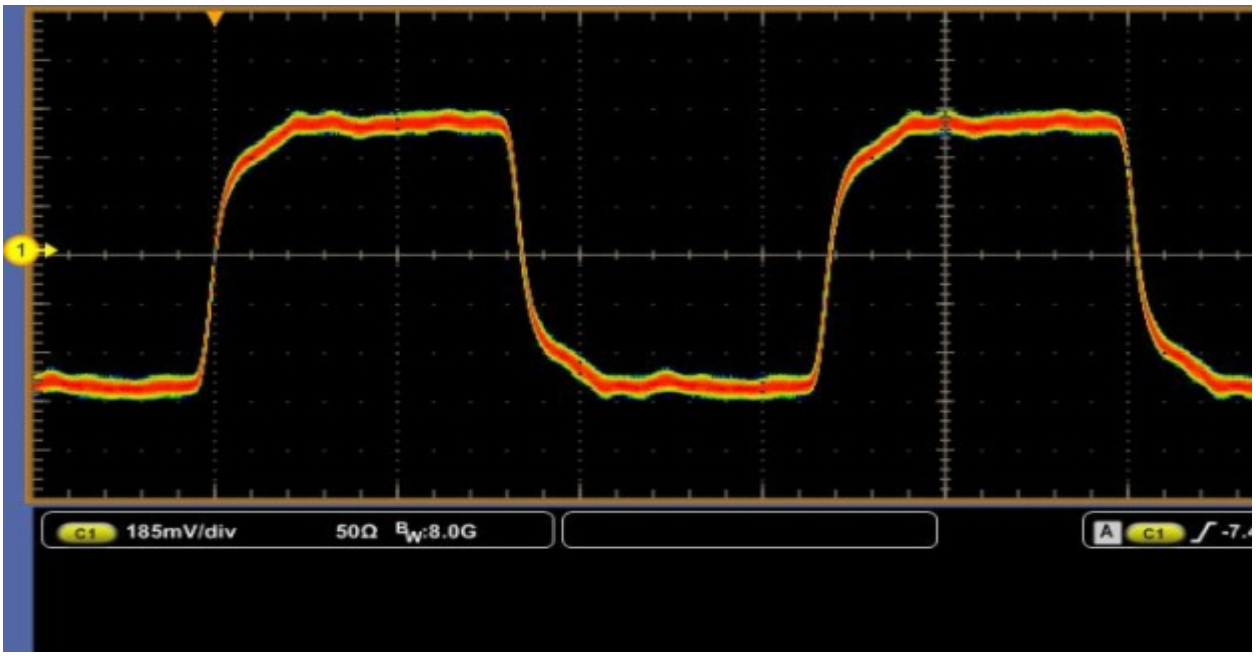
Return to Test Summary

7-8 : Max Duty Cycle : CK

Results

Spec Range	Meas Value	Tbit	Margin	Result
Max Duty Cycle < 60.0%;	50.49%	336.71ps	9.51%	Pass

Waveform/Plot



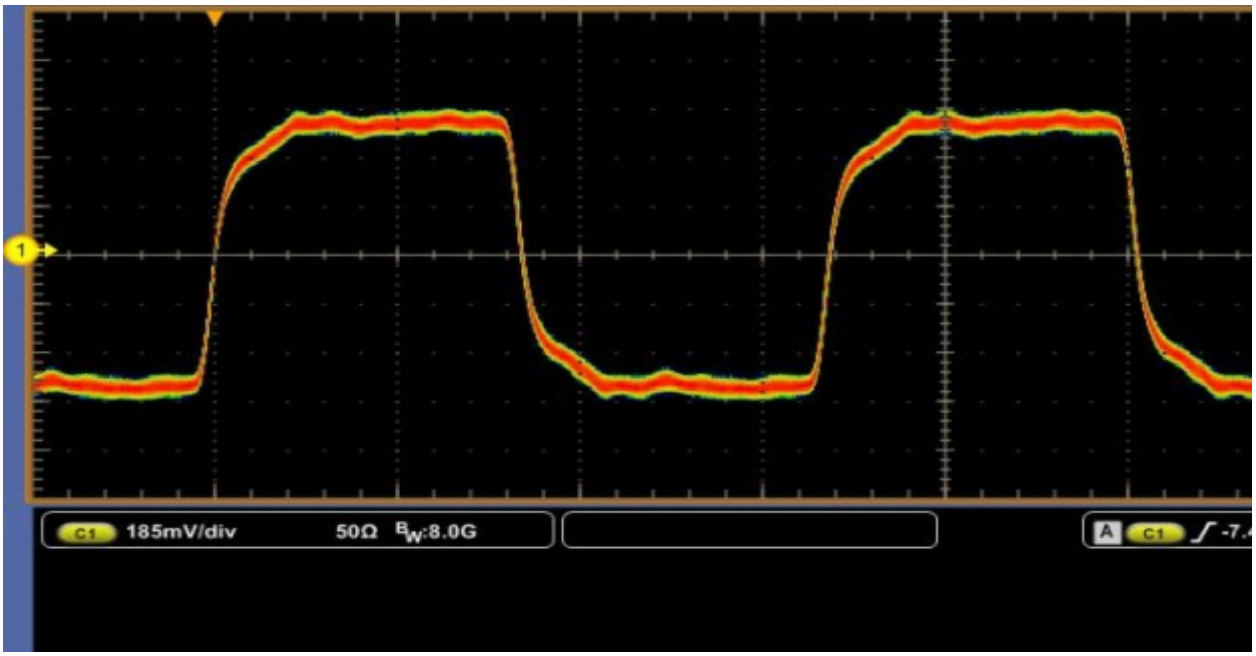
Return to Test Summary

7-8 : Min Duty Cycle : CK

Results

Spec Range	Meas Value	Tbit	Margin	Result
40.0% < Min Duty Cycle;	49.6%	336.71ps	9.6%	Pass

Waveform/Plot



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