Comparison test case study using Zebax ZX200 vs. Agilent N1080A HDMI test fixture (aka. Test board)

The subsequent pages are full test record using Zebax ZX200 HDMI test fixture

Test Case : **4Kx2K 30 Hz PRN**
HDMI Clock Frequency: **2.96GHz**

Full comparison chart can be found here:

ZX200-vs-Agilent-4Kx2K-ZXTR-ZX200-AC2-N1080A.pdf

Agilent Technologies

HDMI™
HIGH-DEFINITION MULTIMEDIA INTERFACE

HDMI Test Report

Overall Results:0 of 20 Tests Failed

Test Configuration Details	
Device Description	
Device Name	Quantum 804A
Comments	Zebax fixture 3 4kx2k 30Hz PRN run 1
Device ID	Transmitter
ConnectionType	4 Connections
HDMI Specification	1.4
Test Fixture Type	Other
Test Session Details	
Infiniium SW Version	05.71.0000
Infiniium Model Number	DSO81204B
Infiniium Serial Number	MY46002010
Application SW Version	1.03.9002
Last Test Date	3/29/2013 10:39:58 AM

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	7-9: Clock Jitter	164mTbit	34.4 %	VALUE <= 250mTbit
✓	0	1	7-10: D0 - Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D0 - Data Jitter	205m	31.7 %	<=0.3Tbit
✓	0	1	7-10: D1 - Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D1 - Data Jitter	207m	31.0 %	<=0.3Tbit
✓	0	1	7-10: D2 - Mask Test	0.000	50.0 %	No Mask Failures
✓	0	1	7-10: D2 - Data Jitter	193m	35.7 %	<=0.3Tbit
✓	0	1	7-4: Clock Rise Time	167.830ps	123.8 %	VALUE >= 75.000ps
✓	0	1	7-4: Clock Fall Time	178.160ps	137.5 %	VALUE >= 75.000ps
✓	0	1	7-4: D0 - Rise Time	93.570ps	24.8 %	VALUE >= 75.000ps
✓	0	1	7-4: D0 - Fall Time	91.620ps	22.2 %	VALUE >= 75.000ps
✓	0	1	7-4: D1 - Rise Time	94.190ps	25.6 %	VALUE >= 75.000ps
✓	0	1	7-4: D1 - Fall Time	89.400ps	19.2 %	VALUE >= 75.000ps
✓	0	1	7-4: D2 - Rise Time	92.230ps	23.0 %	VALUE >= 75.000ps
✓	0	1	7-4: D2 - Fall Time	94.290ps	25.7 %	VALUE >= 75.000ps
✓	0	1	7-8: Clock Duty Cycle(Minimum)	49.440	23.6 %	>=40%
✓	0	1	7-8: Clock Duty Cycle(Maximum)	50.370	16.1 %	<=60%
✓	0	1	7-6: Inter-Pair Skew - D0/D1	600µTpixel	49.8 %	-200mTpixel <= VALUE <= 200mTpixel
✓	0	1	7-6: Inter-Pair Skew - D0/D2	500µTpixel	49.8 %	-200mTpixel <= VALUE <= 200mTpixel
✓	0	1	7-6: Inter-Pair Skew - D1/D2	100µTpixel	50.0 %	-200mTpixel <= VALUE <= 200mTpixel

Report Detail

7-9: Clock Jitter

Reference: Test ID 7-9

Test Summary: Pass

Test Description: | 4 Channels Connection Model: TMDS differential clock jitter must not exceed 0.25*Tbit, relative to the ideal Recovery Clock. For compliance, the DUT should output 27MHz(or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz for testing.

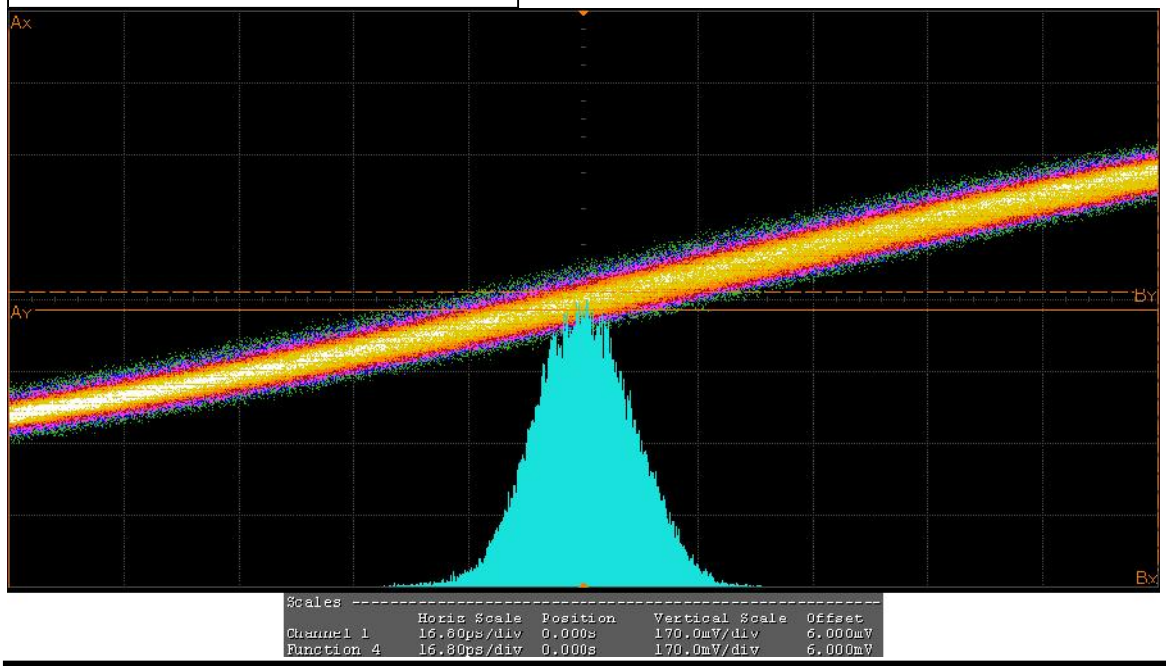
Test Limits: <= 250mTbit | **Clock Jitter** 164mTbit

Result Details

Test Frequency(MHz) 297.081 | **# Edges** 16.000000000M | **Tbit(ps)** 336.609 | **Clock Jitter(ps)** 55.070

Trial 1

Trial 1: Clock Jitter



7-10: D0 - Mask Test

Reference: Test ID 7-10

Test Summary: Pass

Test Description: | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Test Limits: No Mask Failures | **Total # failures** 0.000

Result Details

Maximum Margin 0.000000000000s | **Maximum Margin (Vertical)** 0.000000000000V | **Test Frequency(MHz)** 297.081

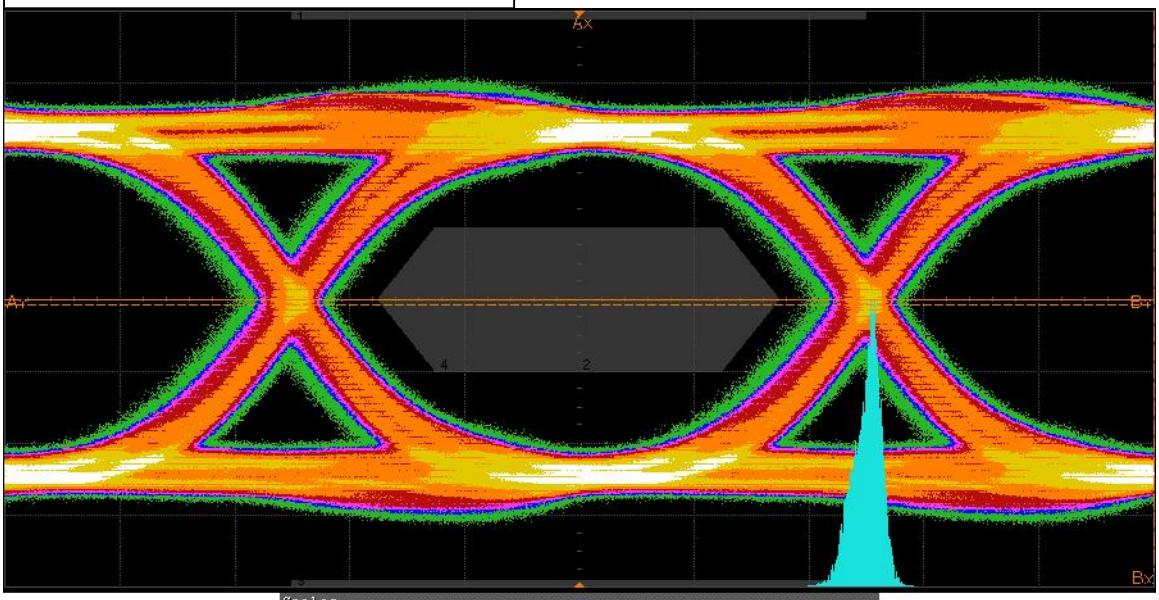
Mask Moved(ps) 0.000 | **# Acquisitions Point** 16.000000000M | **Tbit(ps)** 336.725 | **RightJitterData(Tbit)** 205m

LeftJitterData(Tbit) 202m | **RightJitterData(ps)** 68.900 | **LeftJitterData(ps)** 68.150 | **Differential Swing Voltage(V)** 945m

Mask Revision RevB

Trial 1

Trial 1: Total # failures



7-10: D0 - Data Jitter

Reference: Test ID 7-10

Test Summary: Pass

Test Description: For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Test Limits: <=0.3Tbit **TbitCheck** 205m

Result Details

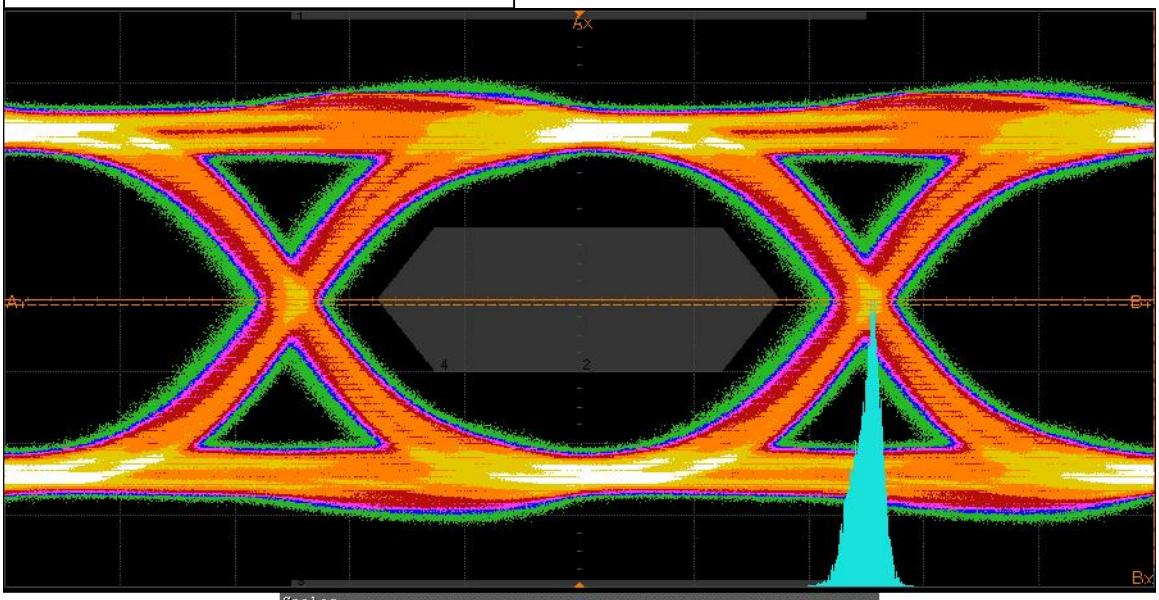
Test Frequency(MHz) 297.081 **Mask Moved(ps)** 0.000 **# Acquisitions Point** 16.000000000M **Tbit(ps)** 336.725

RightJitterData(Tbit) 205m **LeftJitterData(Tbit)** 202m **RightJitterData(ps)** 68.900 **LeftJitterData(ps)** 68.150

Differential Swing Voltage(V) 945m **Mask Revision** RevB

Trial 1

Trial 1: TbitCheck



7-10: D1 - Mask Test

Reference: Test ID 7-10

Test Summary: Pass

Test Description: | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

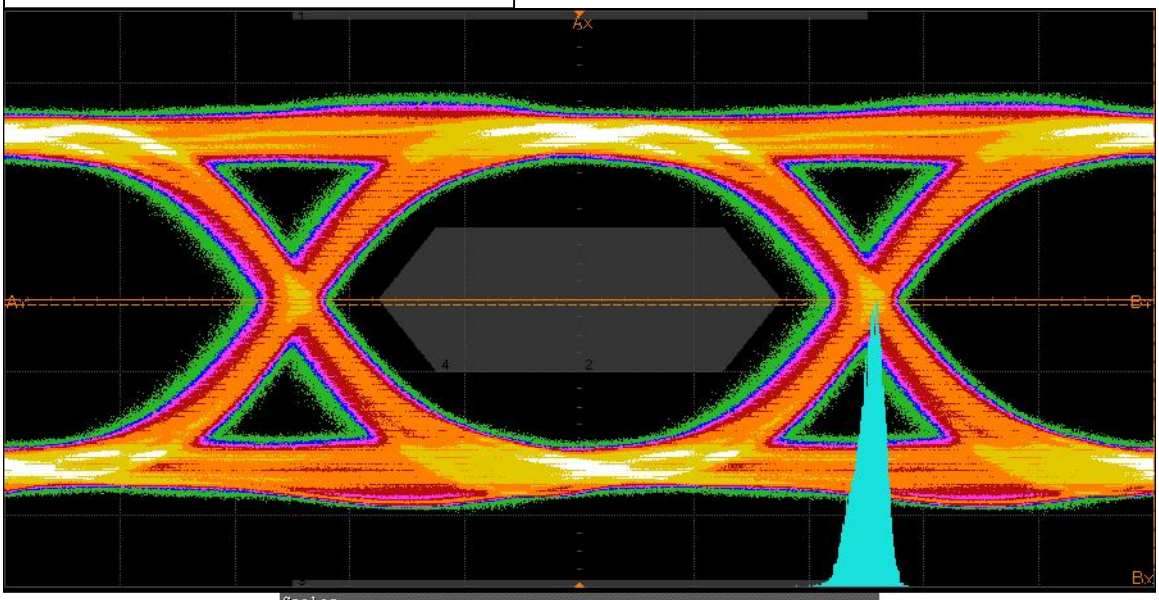
Test Limits: No Mask Failures | **Total # failures** 0.000

Result Details

Maximum Margin 0.000000000000s	**Maximum Margin (Vertical)** 0.000000000000V	**Test Frequency(MHz)** 297.081	
Mask Moved(ps) 0.000	**# Acquisitions Point** 16.000000000M	**Tbit(ps)** 336.688	**RightJitterData(Tbit)** 207m
LeftJitterData(Tbit) 205m	**RightJitterData(ps)** 69.650	**LeftJitterData(ps)** 68.900	**Differential Swing Voltage(V)** 917m
Mask Revision RevB			

Trial 1

Trial 1: Total # failures



7-10: D1 - Data Jitter

Reference: Test ID 7-10

Test Summary: Pass

Test Description: | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Test Limits: <=0.3Tbit **TbitCheck** 207m

Result Details

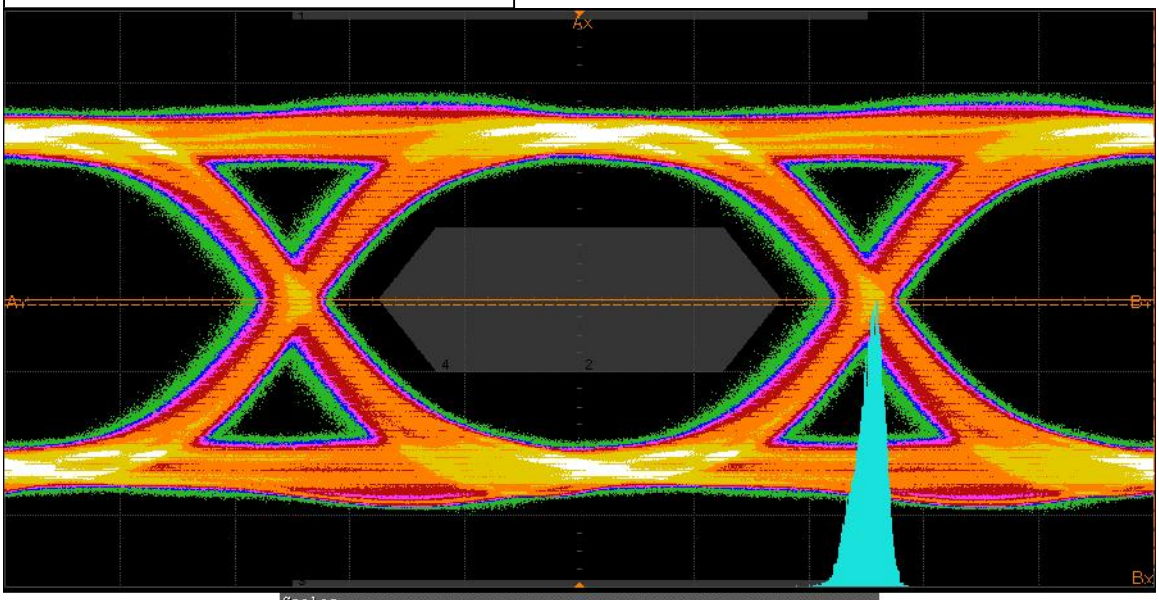
Test Frequency(MHz) 297.081 **Mask Moved(ps)** 0.000 **# Acquisitions Point** 16.000000000M **Tbit(ps)** 336.688

RightJitterData(Tbit) 207m **LeftJitterData(Tbit)** 205m **RightJitterData(ps)** 69.650 **LeftJitterData(ps)** 68.900

Differential Swing Voltage(V) 917m **Mask Revision** RevB

Trial 1

Trial 1: TbitCheck



7-10: D2 - Mask Test

Reference: Test ID 7-10

Test Summary: Pass

Test Description: | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Test Limits: No Mask Failures | **Total # failures** 0.000

Result Details

Maximum Margin 0.000000000000s | **Maximum Margin (Vertical)** 0.000000000000V | **Test Frequency(MHz)** 297.081

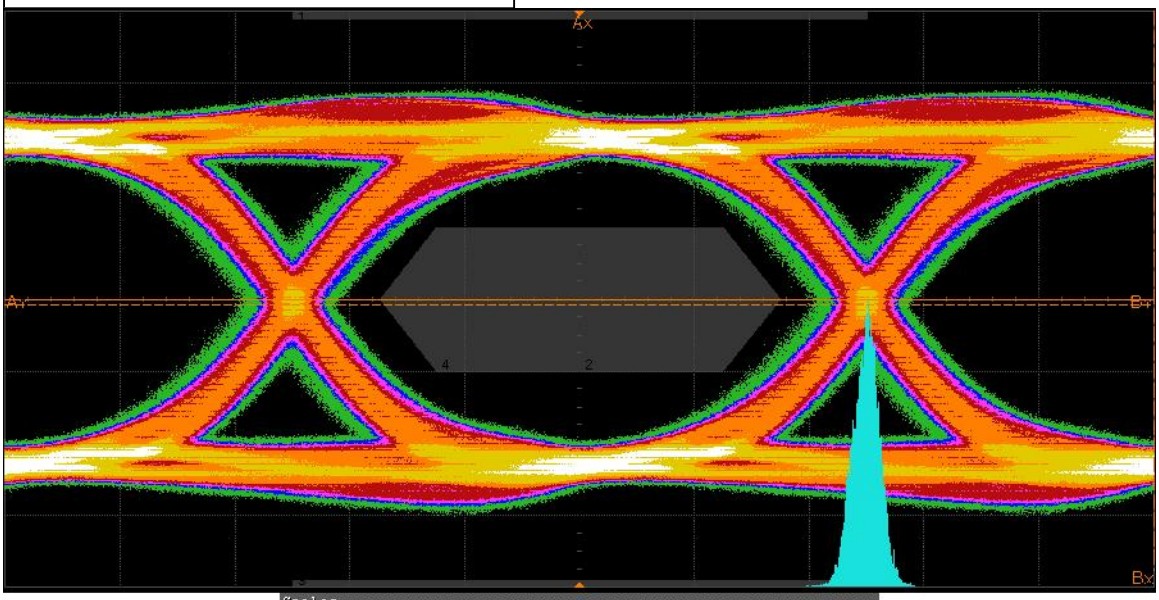
Mask Moved(ps) 0.000 | **# Acquisitions Point** 16.000000000M | **Tbit(ps)** 336.694 | **RightJitterData(Tbit)** 193m

LeftJitterData(Tbit) 193m | **RightJitterData(ps)** 65.150 | **LeftJitterData(ps)** 65.150 | **Differential Swing Voltage(V)** 901m

Mask Revision RevB

Trial 1

Trial 1: Total # failures



7-10: D2 - Data Jitter

Reference: Test ID 7-10

Test Summary: Pass

Test Description: | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Test Limits: <=0.3Tbit **TbitCheck** 193m

Result Details

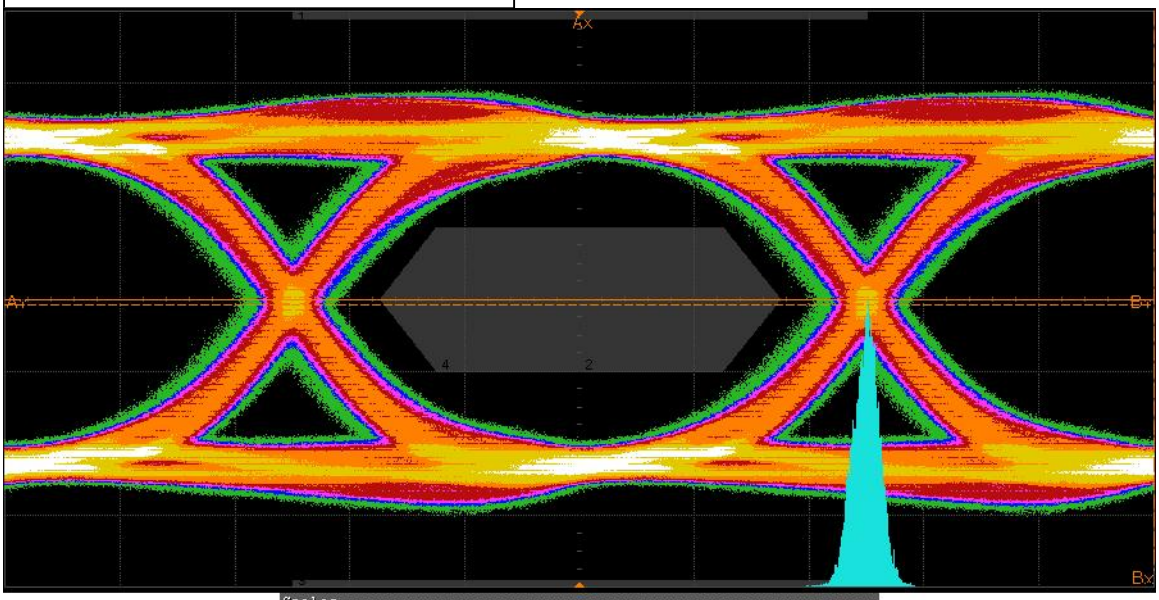
Test Frequency(MHz) 297.081 **Mask Moved(ps)** 0.000 **# Acquisitions Point** 16.000000000M **Tbit(ps)** 336.694

RightJitterData(Tbit) 193m **LeftJitterData(Tbit)** 193m **RightJitterData(ps)** 65.150 **LeftJitterData(ps)** 65.150

Differential Swing Voltage(V) 901m **Mask Revision** RevB

Trial 1

Trial 1: TbitCheck



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	67.40ps/div	0.000s	200.0mV/div	-16.00mV
Channel 4	67.40ps/div	0.000s	200.0mV/div	-8.700mV

✓ 7-4: Clock Rise Time

Reference: Test ID 7-4

Test Summary: Pass

Test Description: 4 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

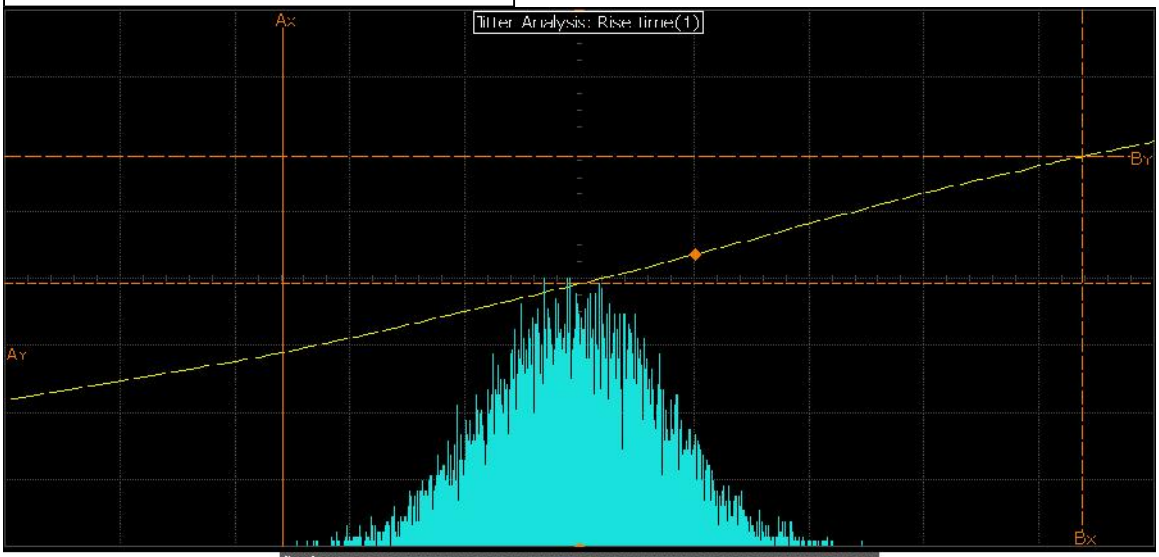
Test Limits: >= 75.000ps | **Raw Clock Transition Time** 167.830ps

Result Details

Test Frequency(MHz) 297.081 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000 | **# Edges** 10.997000k

Trial 1

Trial 1: Raw Clock Transition Time



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	23.80ps/div	0.000s	200.0mV/div	-16.00mV

Markers

	Source	X Position	Y Position
A	Channel 1	-61.000000000000ps	-236.30mV
B	Channel 1	103.000000000000ps	947.772mV

✓ 7-4: Clock Fall Time

Reference: Test ID 7-4

Test Summary: Pass | Test Description: | 4 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

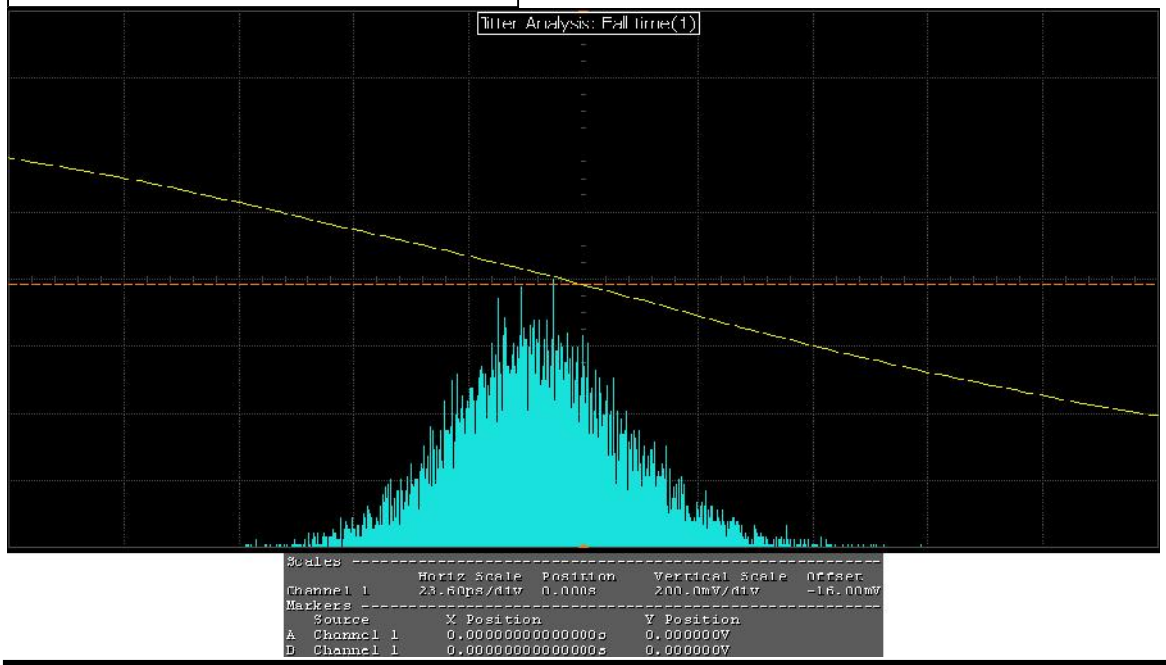
Test Limits: >= 75.000ps | **Raw Clock Transition Time** 178.160ps

Result Details

Test Frequency(MHz) 297.081 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000 | **# Edges** 10.996000k

Trial 1

Trial 1: Raw Clock Transition Time



7-4: D0 - Rise Time

Reference: Test ID 7-4

Test Summary: Pass | Test Description: | The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >= 75.000ps | **Transition Time** 93.570ps

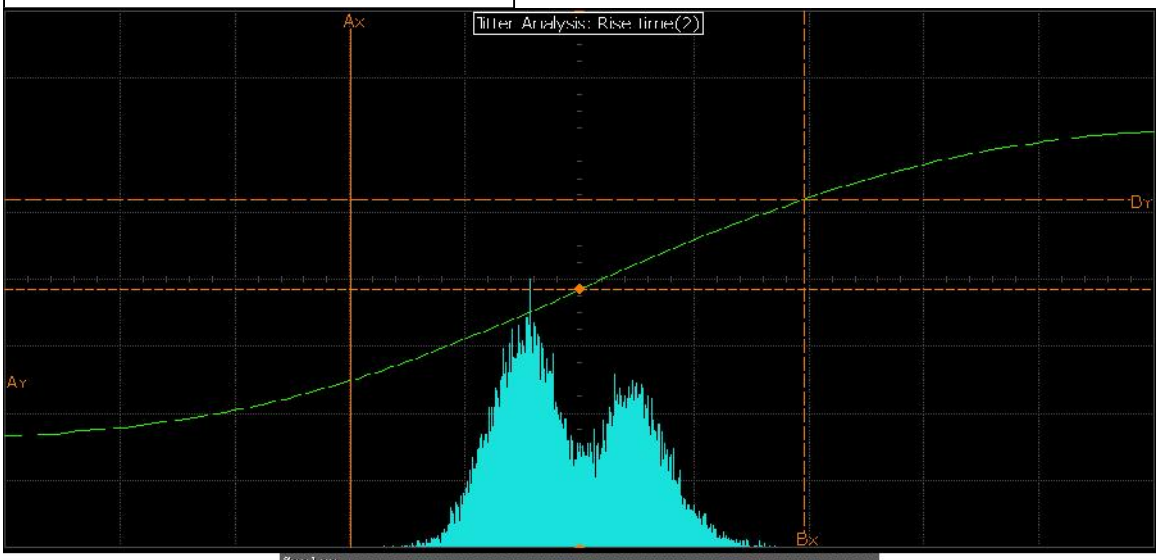
Result Details

Test Frequency(MHz) 297.081 | **Data Lane A** D0 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000

#Edge 25.514000k

Trial 1

Trial 1: Transition Time



7-4: D0 - Fall Time

Reference: Test ID 7-4

Test Summary: Pass

Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >= 75.000ps | **Transition Time** 91.620ps

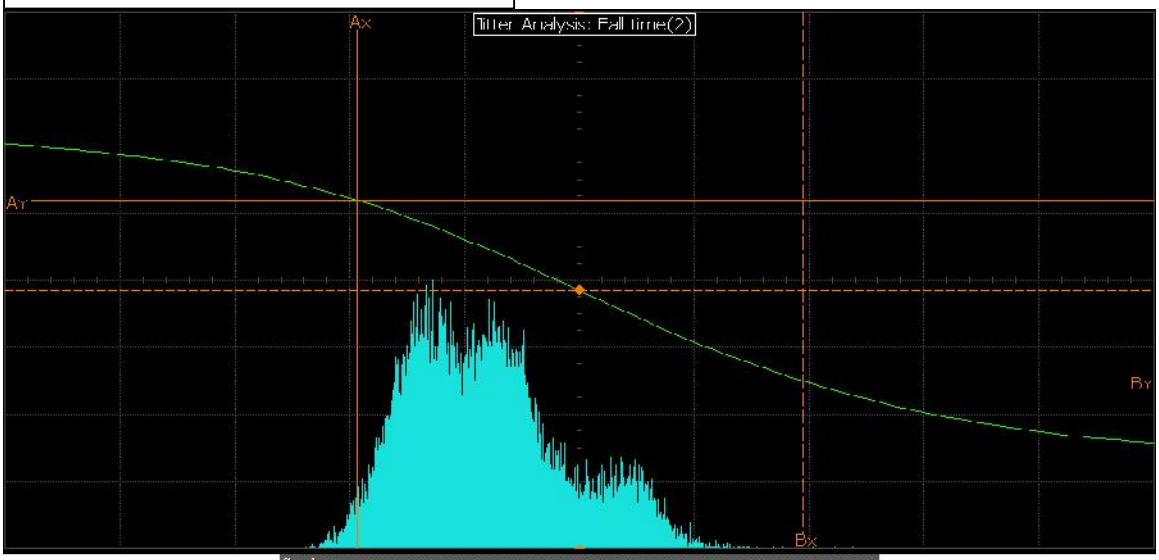
Result Details

Test Frequency(MHz) 297.081 | **Data Lane A** D0 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000

#Edge 25.871000k

Trial 1

Trial 1: Transition Time



7-4: D1 - Rise Time

Reference: Test ID 7-4

Test Summary: Pass | Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >= 75.000ps | **Transition Time** 94.190ps

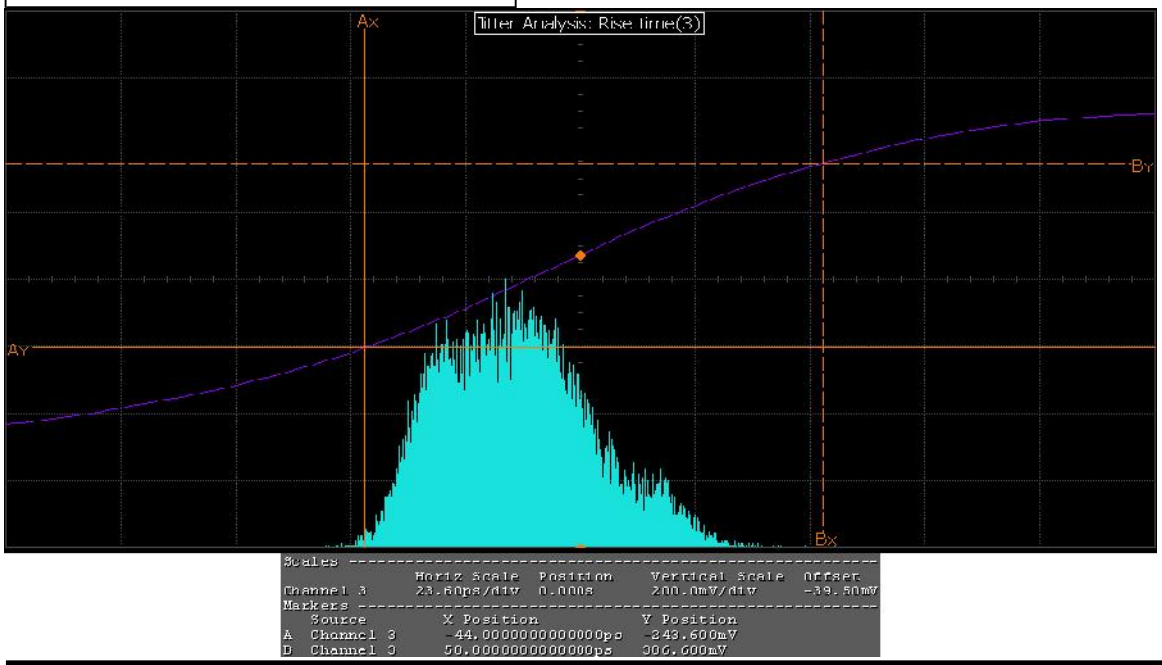
Result Details

Test Frequency(MHz) 297.081 | **Data Lane A** D0 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000

#Edge 24.764000k

Trial 1

Trial 1: Transition Time



7-4: D1 - Fall Time

Reference: Test ID 7-4

Test Summary: Pass | Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >= 75.000ps | **Transition Time** 89.400ps

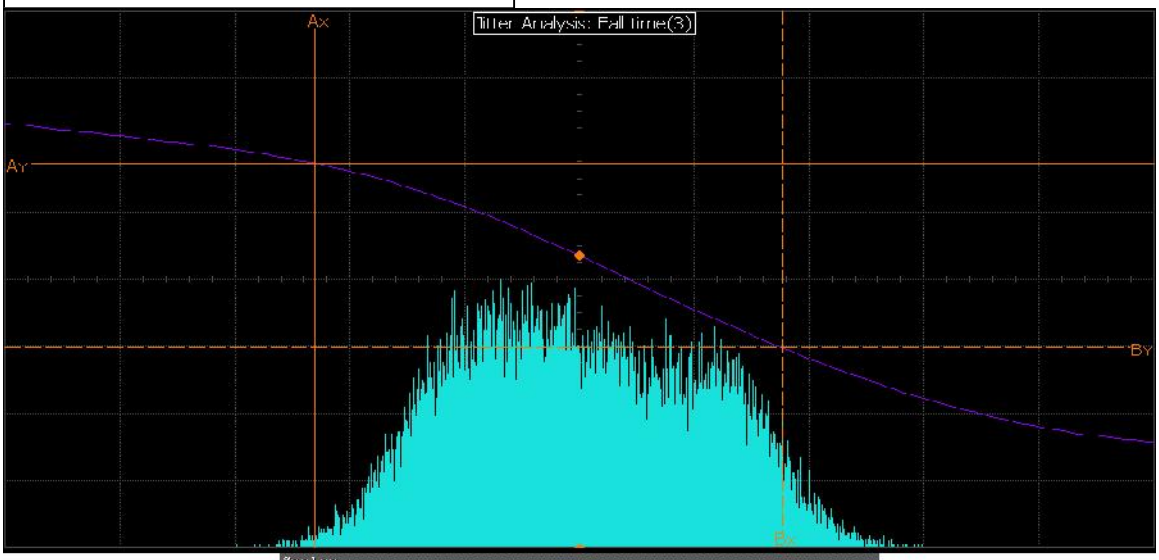
Result Details

Test Frequency(MHz) 297.081 | **Data Lane A** D0 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000

#Edge 25.726000k

Trial 1

Trial 1: Transition Time



7-4: D2 - Rise Time

Reference: Test ID 7-4

Test Summary: Pass

Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >= 75.000ps | **Transition Time** 92.230ps

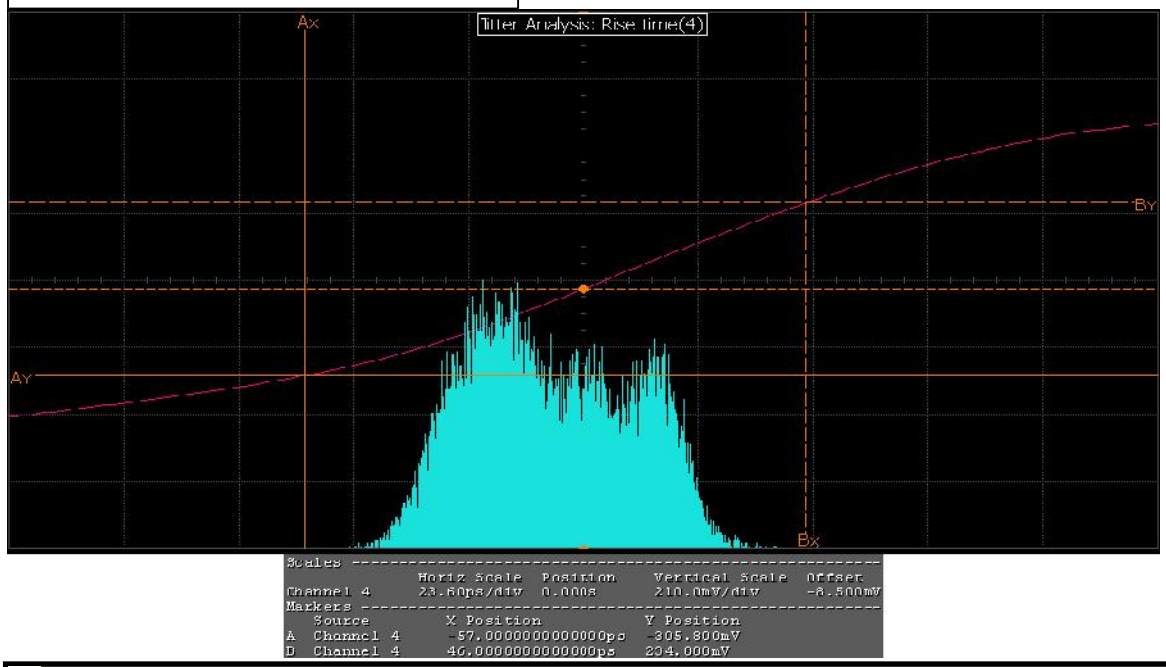
Result Details

Test Frequency(MHz) 297.081 | **Data Lane A** D0 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000

#Edge 25.737000k

Trial 1

Trial 1: Transition Time



7-4: D2 - Fall Time

Reference: Test ID 7-4

Test Summary: Pass

Test Description: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >= 75.000ps **Transition Time** 94.290ps

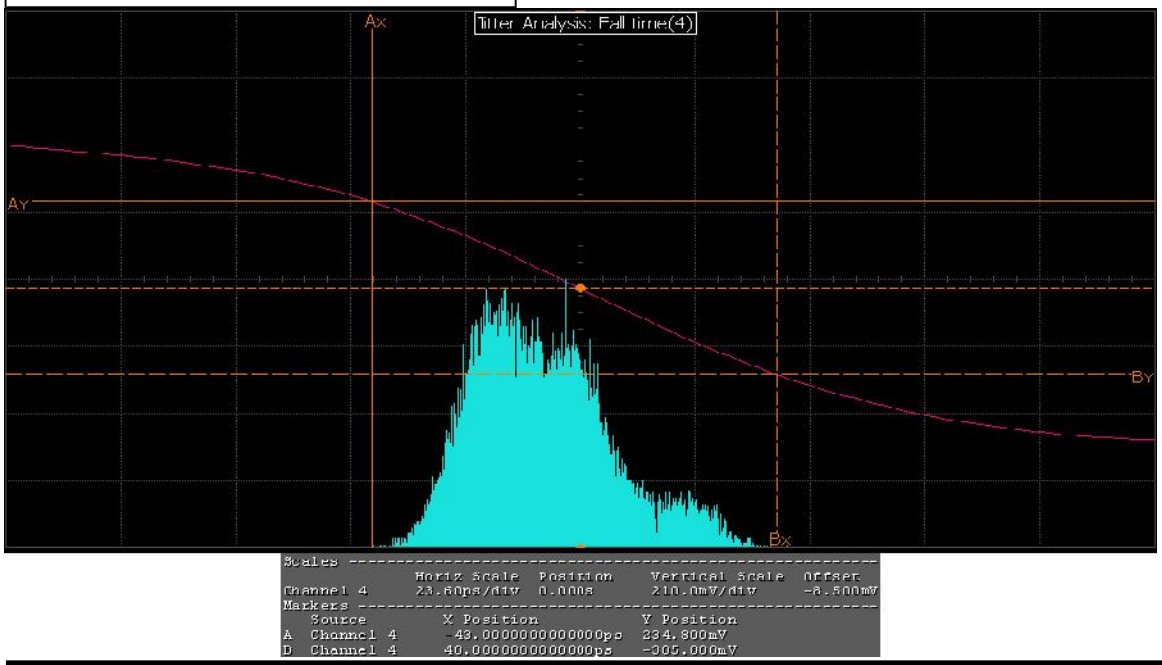
Result Details

Test Frequency(MHz) 297.081 **Data Lane A** D0 **Upper Threshold(%)** 80.000 **Lower Threshold(%)** 20.000

#Edge 24.862000k

Trial 1

Trial 1: Transition Time



7-8: Clock Duty Cycle(Minimum)

Reference: Test ID 7-8

Test Summary: Pass

Test Description: 4 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

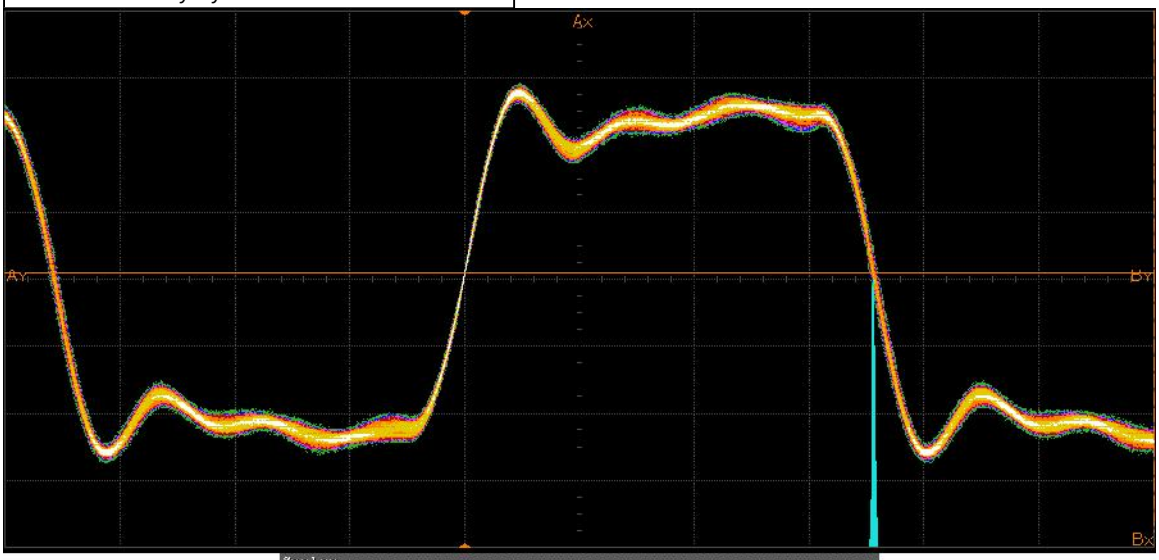
Test Limits: >=40% **Clock Duty Cycle Minimum** 49.440

Result Details

Test Frequency(MHz) 297.081 **# Edges** 10.000000k **TdutyMIN(ns)** 1.664

Trial 1

Trial 1: Clock Duty Cycle Minimum



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	471.0ps/div	471.0ps	200.0mV/div	-16.00mV

Markers

	Source	X Position	Y Position
A	Channel 1	0.000000000000000s	0.000000V
B	Channel 1	0.000000000000000s	0.000000V

7-8: Clock Duty Cycle(Maximum)

Reference: Test ID 7-8

Test Summary: Pass

Test Description: 4 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

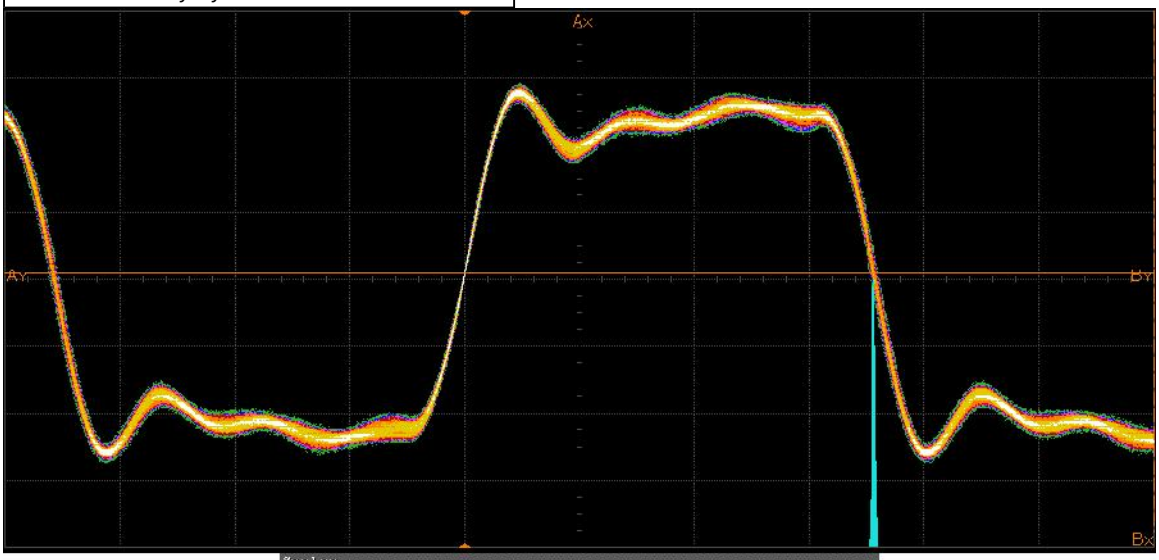
Test Limits: <=60% **Clock Duty Cycle Maximum** 50.370

Result Details

Test Frequency(MHz) 297.081 **# Edges** 10.000000k **TdutyMAX(ns)** 1.696

Trial 1

Trial 1: Clock Duty Cycle Maximum



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	471.0ps/div	471.0ps	200.0mV/div	-16.00mV

Markers

	Source	X Position	Y Position
A	Channel 1	0.000000000000000s	0.000000V
B	Channel 1	0.000000000000000s	0.000000V

7-6: Inter-Pair Skew - D0/D1

Reference: Test ID 7-6

Test Summary: Pass | Test Description: | Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: [-200mTpixel to 200mTpixel] **Data - Data Inter-Pair Skew** 600µTpixel

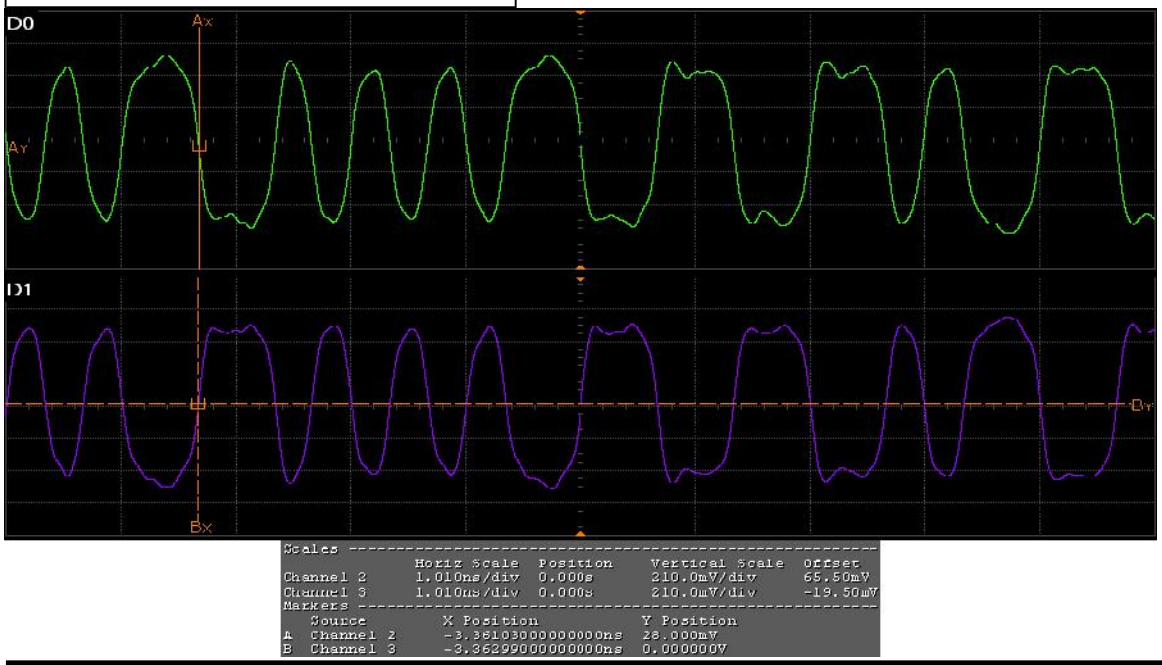
Result Details

Test Frequency(MHz) 297.081 **Data Lane A** N/A **Data Lane B** N/A **Data - Data Inter-Pair Skew(ps)** 1.960

Triggered Pattern 20

Trial 1

Trial 1: Data - Data Inter-Pair Skew



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	1.010ns/div	0.000s	210.0mV/div	65.50mV
Channel 3	1.010ns/div	0.000s	210.0mV/div	-19.50mV

Markers

	Source	X Position	Y Position
A	Channel 2	-3.361030000000000ns	28.000mV
B	Channel 3	-3.362990000000000ns	0.000000V

7-6: Inter-Pair Skew - D0/D2

Reference: Test ID 7-6

Test Summary: Pass | Test Description: | Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: [-200mTpixel to 200mTpixel] **Data - Data Inter-Pair Skew** 500µTpixel

Result Details

Test Frequency(MHz) 297.081 **Data Lane A** N/A **Data Lane B** N/A **Data - Data Inter-Pair Skew(ps)** 1.700

Triggered Pattern 20

Trial 1

Trial 1: Data - Data Inter-Pair Skew

Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 2	1.010ns/div	0.000s	210.0mV/div	48.50mV
Channel 4	1.010ns/div	0.000s	210.0mV/div	-6.000mV

Markers

	Source	X Position	Y Position
A	Channel 2	-3.37420000000000ns	41.000mV
B	Channel 1	-3.37250000000000ns	-3.000mV

✓ 7-6: Inter-Pair Skew - D1/D2

Reference: Test ID 7-6

Test Summary: Pass

Test Description: | Inter-pair skew must not exceed 0.20*Tpixel. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: [-200mTpixel to 200mTpixel] **Data - Data Inter-Pair Skew** 100µTpixel

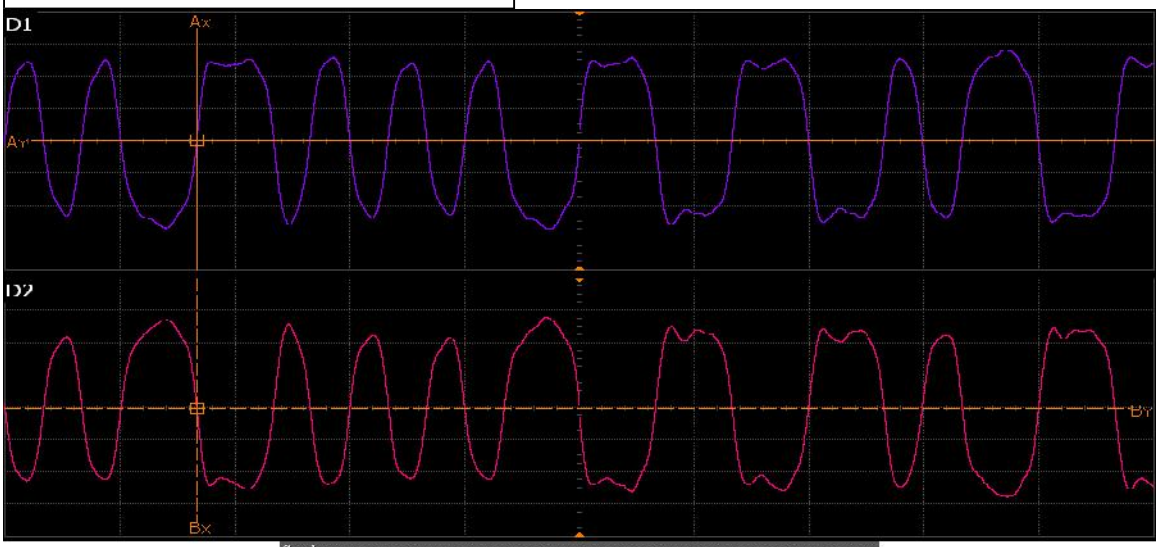
Result Details

Test Frequency(MHz) 296.953 **Data Lane A** N/A **Data Lane B** N/A **Data - Data Inter-Pair Skew(ps)** 340m

Triggered Pattern 20

Trial 1

Trial 1: Data - Data Inter-Pair Skew



Scales

	Horiz Scale	Position	Vertical Scale	Offset
Channel 3	1.010ns/div	0.000s	200.0mV/div	-1.500mV
Channel 4	1.010ns/div	0.000s	200.0mV/div	-6.000mV

Markers

	Source	X Position	Y Position
A	Channel 3	-3.36986000000000ns	0.000000V
B	Channel 1	-3.37020000000000ns	-10.000mV

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