

Comparison test case study using Zebax ZX200 vs. Agilent N1080A HDMI test fixture (aka. Test board)

The subsequent pages are full test record using Agilent N1080A HDMI test fixture

Test Case : **4Kx2K 30 Hz PRN**
HDMI Clock Frequency: **2.96GHz**

Full comparison chart can be found here:

ZX200-vs-Agilent-4Kx2K-ZXTR-ZX200-AC2-N1080A.pdf



HDMI Test Report

Overall Results: 0 of 20 Tests Failed

Test Configuration Details	
Device Description	
Device Name	Quantum 804A
Comments	Agilent Fixture 4K X2K 30 Hz PRN output 1
Device ID	Transmitter
ConnectionType	4 Connections
HDMI Specification	1.4
Test Fixture Type	N1080A
Test Session Details	
Infiniium SW Version	05.71.0000
Infiniium Model Number	DSO81204B
Infiniium Serial Number	MY46002010
Application SW Version	1.03.9002
Last Test Date	4/1/2013 10:59:52 AM

Summary of Results

Margin Thresholds	
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
✓	0	1	<u>7-9: Clock Jitter</u>	181mTbit	27.6 %	VALUE <= 250mTbit
✓	0	1	<u>7-10: D0 - Mask Test</u>	0.000	50.0 %	No Mask Failures
✓	0	1	<u>7-10: D0 - Data Jitter</u>	202m	32.7 %	<=0.3Tbit
✓	0	1	<u>7-10: D1 - Mask Test</u>	0.000	50.0 %	No Mask Failures
✓	0	1	<u>7-10: D1 - Data Jitter</u>	200m	33.3 %	<=0.3Tbit
✓	0	1	<u>7-10: D2 - Mask Test</u>	0.000	50.0 %	No Mask Failures
✓	0	1	<u>7-10: D2 - Data Jitter</u>	189m	37.0 %	<=0.3Tbit
✓	0	1	<u>7-4: Clock Rise Time</u>	203.250ps	171.0 %	VALUE >= 75.000ps
✓	0	1	<u>7-4: Clock Fall Time</u>	186.530ps	148.7 %	VALUE >= 75.000ps
✓	0	1	<u>7-4: D0 - Rise Time</u>	94.840ps	26.5 %	VALUE >= 75.000ps
✓	0	1	<u>7-4: D0 - Fall Time</u>	93.580ps	24.8 %	VALUE >= 75.000ps
✓	0	1	<u>7-4: D1 - Rise Time</u>	92.690ps	23.6 %	VALUE >= 75.000ps
✓	0	1	<u>7-4: D1 - Fall Time</u>	90.320ps	20.4 %	VALUE >= 75.000ps
✓	0	1	<u>7-4: D2 - Rise Time</u>	99.130ps	32.2 %	VALUE >= 75.000ps
✓	0	1	<u>7-4: D2 - Fall Time</u>	93.070ps	24.1 %	VALUE >= 75.000ps
✓	0	1	<u>7-8: Clock Duty Cycle(Minimum)</u>	49.420	23.6 %	>=40%
✓	0	1	<u>7-8: Clock Duty Cycle(Maximum)</u>	50.350	16.1 %	<=60%
✓	0	1	<u>7-6: Inter-Pair Skew - D0/D1</u>	4mTpixel	49.0 %	-200mTpixel <= VALUE <= 200mTpixel
✓	0	1	<u>7-6: Inter-Pair Skew - D0/D2</u>	4mTpixel	49.0 %	-200mTpixel <= VALUE <= 200mTpixel
✓	0	1	<u>7-6: Inter-Pair Skew - D1/D2</u>	2mTpixel	49.5 %	-200mTpixel <= VALUE <= 200mTpixel

Report Detail

7-9: Clock Jitter

Reference: Test ID 7-9

Test Summary: Pass **Test Description:** | 4 Channels Connection Model: TMDS differential clock jitter must not exceed $0.25 \times T_{bit}$, relative to the ideal Recovery Clock. For compliance, the DUT should output 27MHz(or 25MHz), 74.25MHz, 148.5MHz, and 222.75MHz for testing.

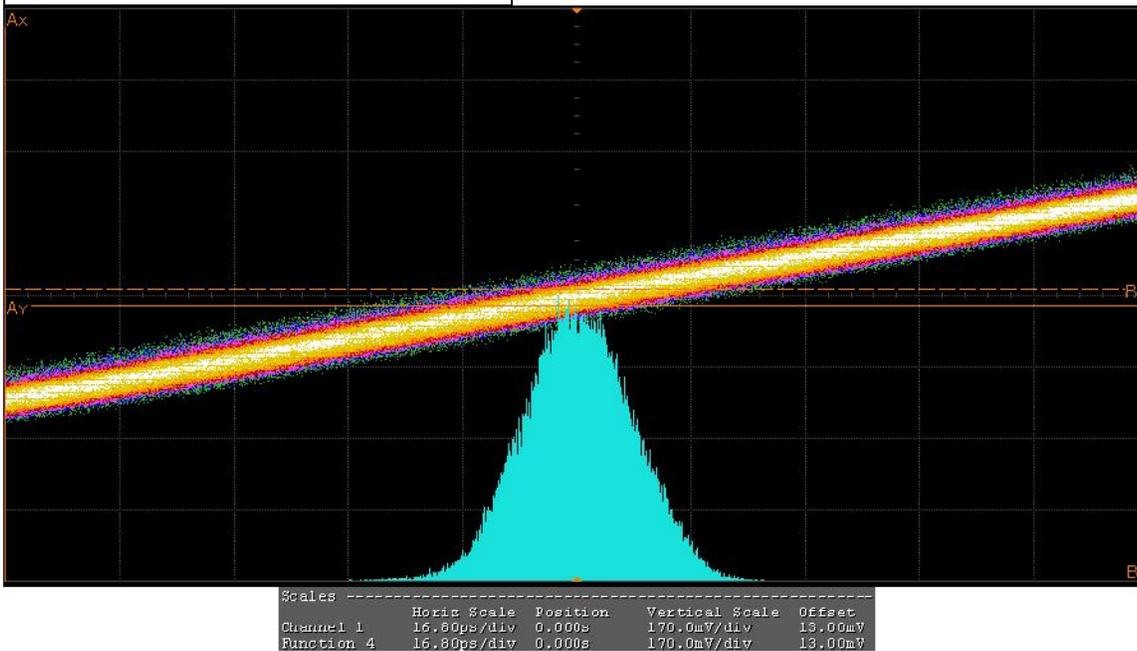
Test Limits: $\leq 250mT_{bit}$ **Clock Jitter** 181mTbit

Result Details

Test Frequency(MHz) 296.966 **# Edges** 16.000000000M **Tbit(ps)** 336.739 **Clock Jitter(ps)** 60.850

Trial 1

Trial 1: Clock Jitter



7-10: D0 - Mask Test

Reference: Test ID 7-10

Test Summary: Pass **Test Description:** | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

Test Limits: No Mask Failures **Total # failures** 0.000

Result Details

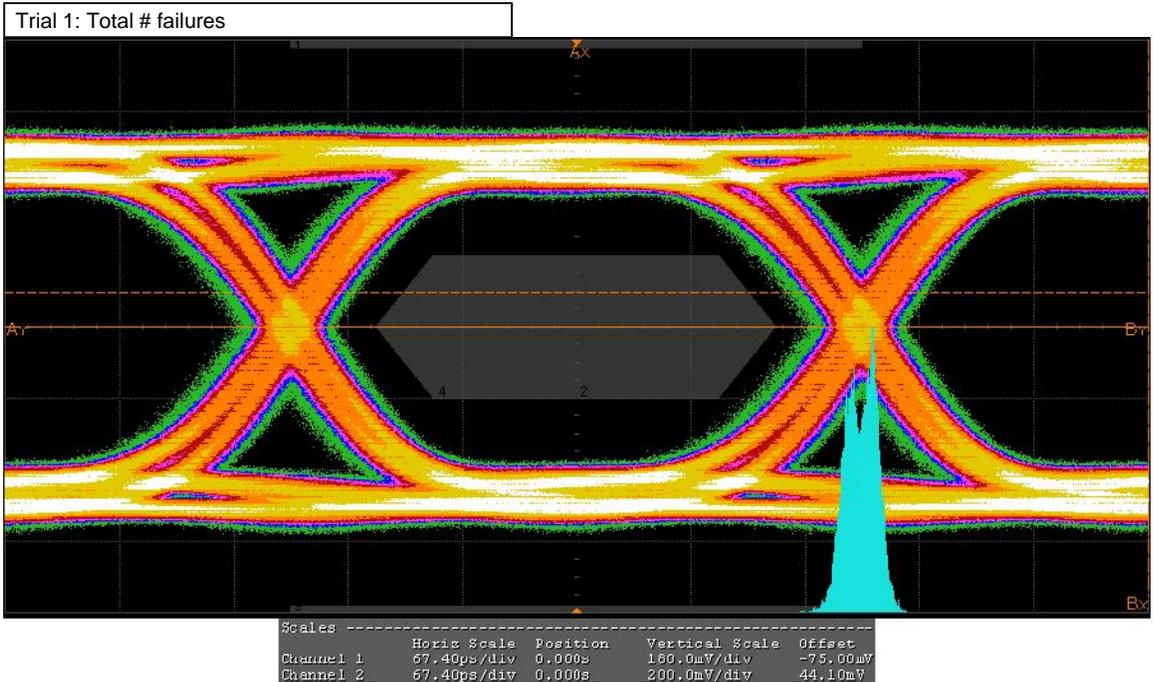
Maximum Margin 0.000000000000s **Maximum Margin (Vertical)** 0.000000000000V **Test Frequency(MHz)** 296.966

Mask Moved(ps) 0.000 **# Acquisitions Point** 16.000000000M **Tbit(ps)** 336.679 **RightJitterData(Tbit)** 202m

LeftJitterData(Tbit) 202m **RightJitterData(ps)** 68.150 **LeftJitterData(ps)** 68.150 **Differential Swing Voltage(V)** 1.003

Mask Revision RevB

Trial 1



✓ 7-10: D0 - Data Jitter Reference: Test ID 7-10

Test Summary: **Pass** | **Test Description:** | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

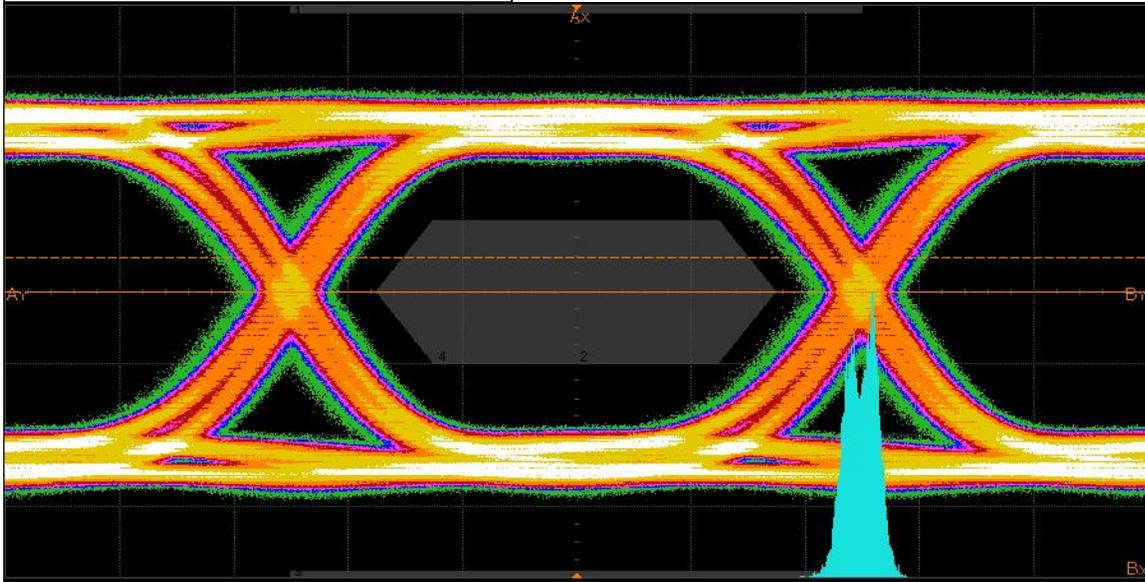
Test Limits: <=0.3Tbit | **TbitCheck** 202m

Result Details

Test Frequency(MHz) 296.966	Mask Moved(ps) 0.000	# Acquisitions Point 16.000000000M	Tbit(ps) 336.679
RightJitterData(Tbit) 202m	LeftJitterData(Tbit) 202m	RightJitterData(ps) 68.150	LeftJitterData(ps) 68.150
Differential Swing Voltage(V) 1.003	Mask Revision RevB		

Trial 1

Trial 1: TbitCheck



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	67.40ps/div	0.000s	180.0mV/div	-75.00mV
Channel 2	67.40ps/div	0.000s	200.0mV/div	44.10mV

✓ 7-10: D1 - Mask Test

Reference: Test ID 7-10

Test Summary: **Pass** | **Test Description:** | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

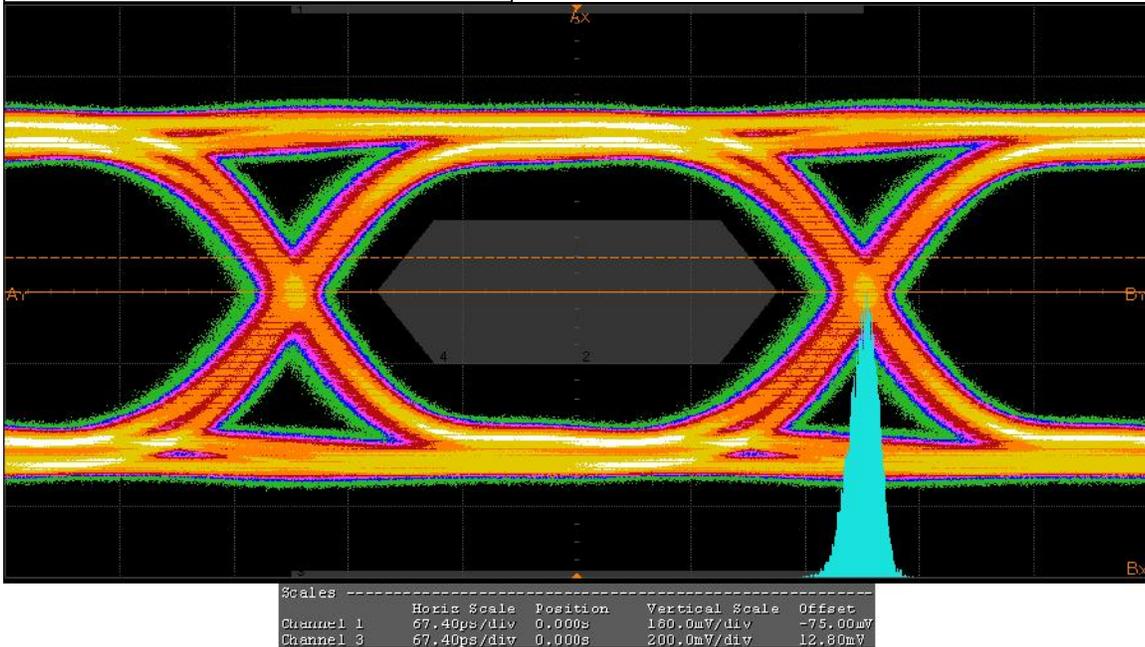
Test Limits: No Mask Failures | **Total # failures** 0.000

Result Details

Maximum Margin 0.000000000000s	Maximum Margin (Vertical) 0.000000000000V	Test Frequency(MHz) 296.966
Mask Moved(ps) 0.000	# Acquisitions Point 16.000000000M	Tbit(ps) 336.678
RightJitterData(Tbit) 200m	LeftJitterData(Tbit) 198m	RightJitterData(ps) 67.400
LeftJitterData(ps) 66.650	Differential Swing Voltage(V) 950m	
Mask Revision RevB		

Trial 1

Trial 1: Total # failures



✓ 7-10: D1 - Data Jitter

Reference: Test ID 7-10

Test Summary: Pass | Test Description: | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at

TP1, which meet the normalized eye diagram requirements.

Test Limits: <=0.3Tbit | TbitCheck 200m

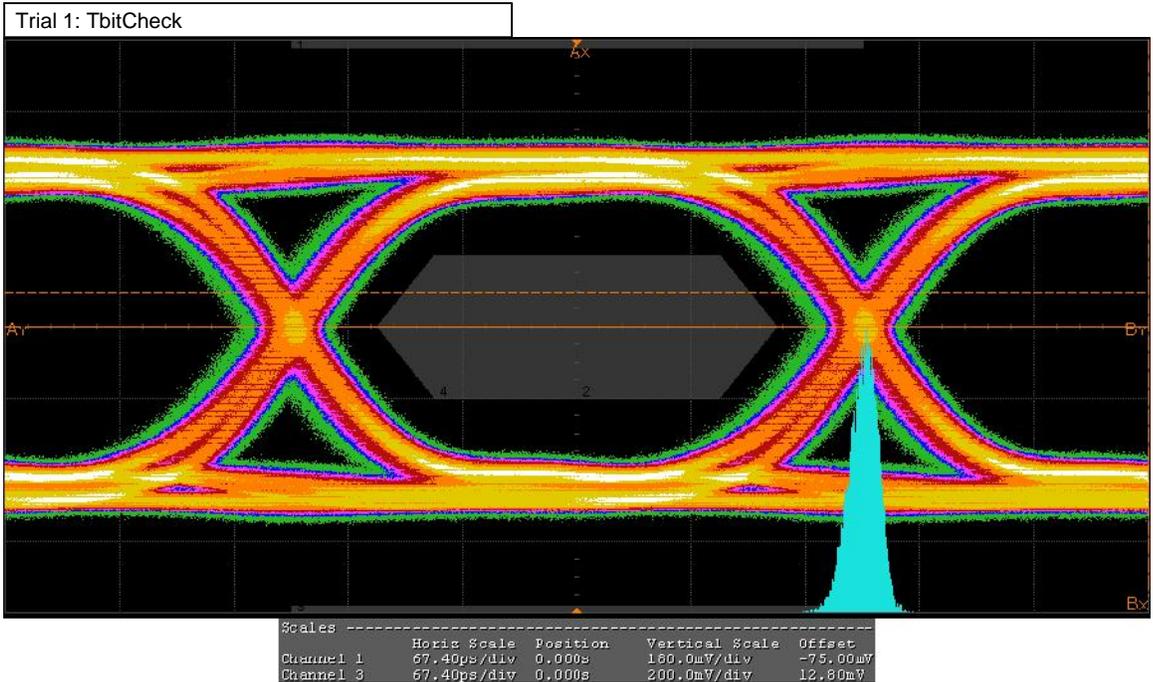
Result Details

Test Frequency(MHz) 296.966 | Mask Moved(ps) 0.000 | # Acquisitions Point 16.000000000M | Tbit(ps) 336.678

RightJitterData(Tbit) 200m | LeftJitterData(Tbit) 198m | RightJitterData(ps) 67.400 | LeftJitterData(ps) 66.650

Differential Swing Voltage(V) 950m | Mask Revision RevB

Trial 1



✓ 7-10: D2 - Mask Test Reference: Test ID 7-10

Test Summary: **Pass** | **Test Description:** | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at TP1, which meet the normalized eye diagram requirements.

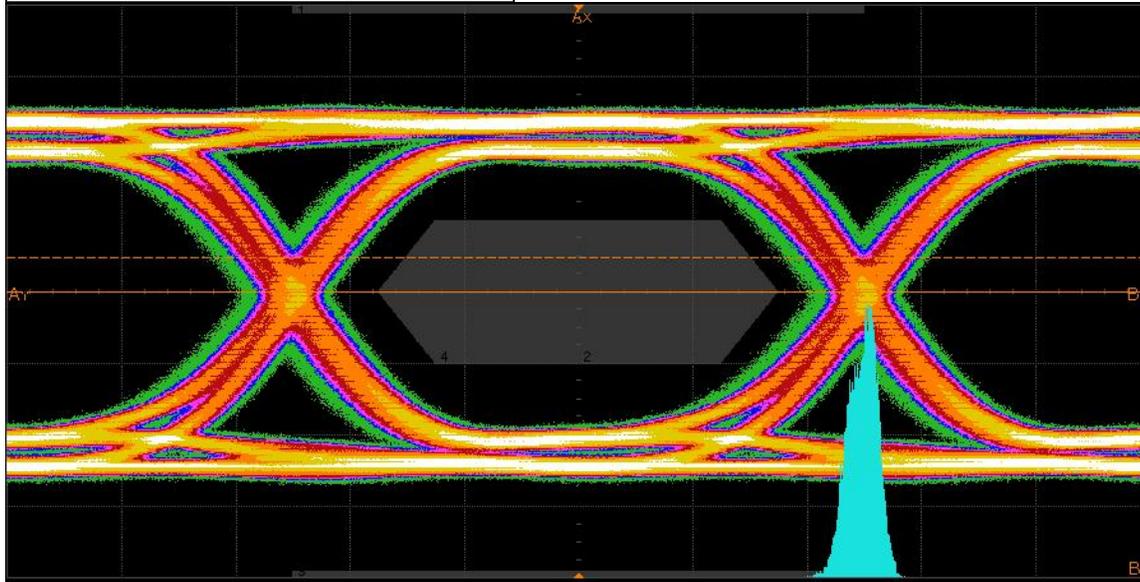
Test Limits: No Mask Failures | **Total # failures** 0.000

Result Details

Maximum Margin 0.000000000000s	Maximum Margin (Vertical) 0.000000000000V	Test Frequency(MHz) 296.966
Mask Moved(ps) 0.000	# Acquisitions Point 16.000000000M	Tbit(ps) 336.689
RightJitterData(Tbit) 189m	LeftJitterData(Tbit) 187m	RightJitterData(ps) 63.660
LeftJitterData(ps) 62.910	Differential Swing Voltage(V) 965m	
Mask Revision RevB		

Trial 1

Trial 1: Total # failures



Channel	Horiz Scale	Position	Vertical Scale	Offset
Channel 1	67.40ps/div	0.000s	100.0mV/div	-75.00mV
Channel 4	67.40ps/div	0.000s	200.0mV/div	-8.700mV

✓ 7-10: D2 - Data Jitter

Reference: Test ID 7-10

Test Summary: **Pass** | **Test Description:** | For all channels under all operating conditions specified in Table 4-11 . The Source shall have output levels at

TP1, which meet the normalized eye diagram requirements.

Test Limits: <=0.3Tbit | **TbitCheck** 189m

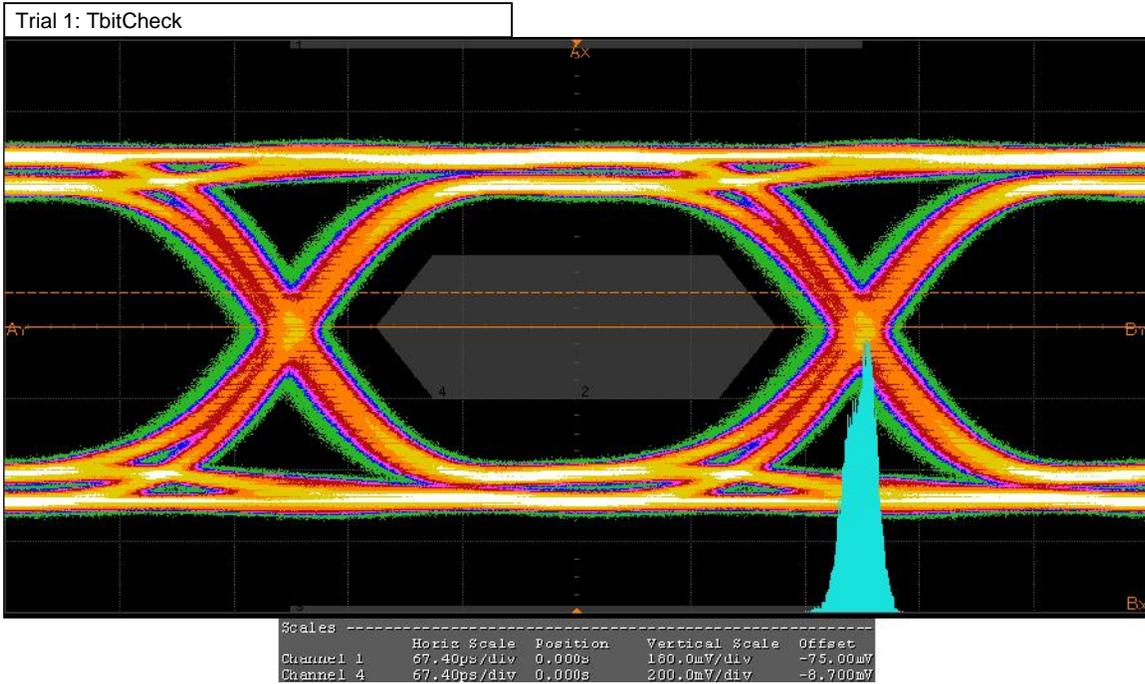
Result Details

Test Frequency(MHz) 296.966 | **Mask Moved(ps)** 0.000 | **# Acquisitions Point** 16.000000000M | **Tbit(ps)** 336.689

RightJitterData(Tbit) 189m | **LeftJitterData(Tbit)** 187m | **RightJitterData(ps)** 63.660 | **LeftJitterData(ps)** 62.910

Differential Swing Voltage(V) 965m | **Mask Revision** RevB

Trial 1



✓ 7-4: Clock Rise Time Reference: Test ID 7-4

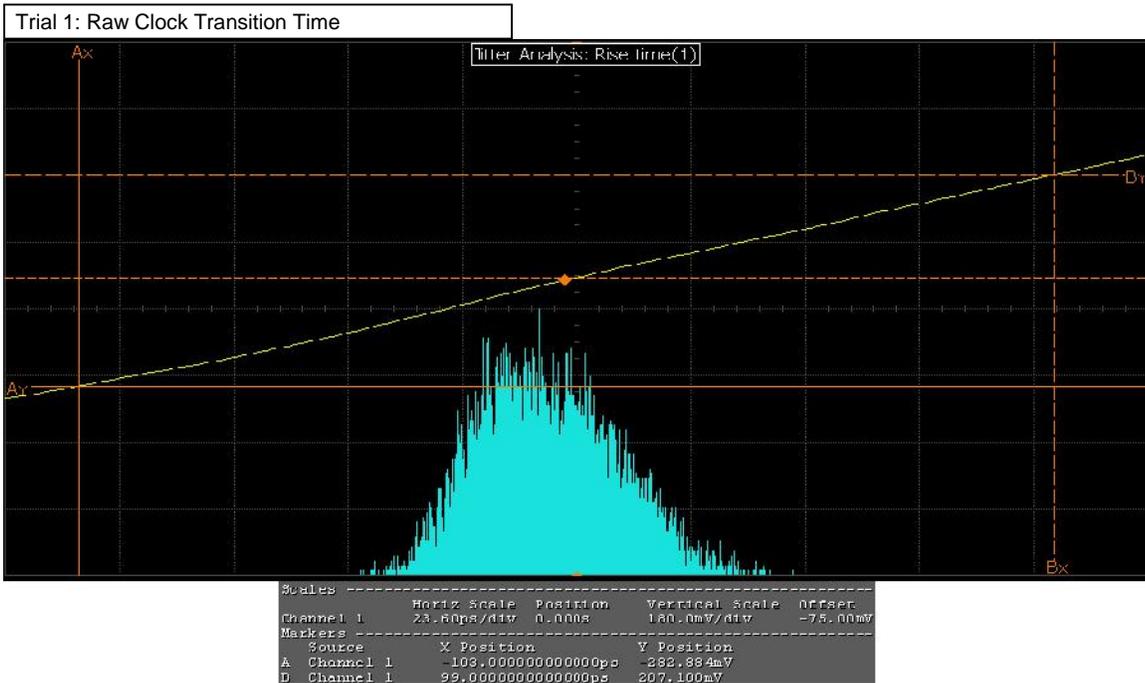
Test Summary: **Pass** | **Test Description:** | 4 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: $\geq 75.000ps$ | **Raw Clock Transition Time** 203.250ps

Result Details

Test Frequency(MHz) 296.966 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000 | **# Edges** 11.000000k

Trial 1



✓ 7-4: Clock Fall Time Reference: Test ID 7-4

Test Summary: Pass **Test Description:** | 4 Channels Connection Model: The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

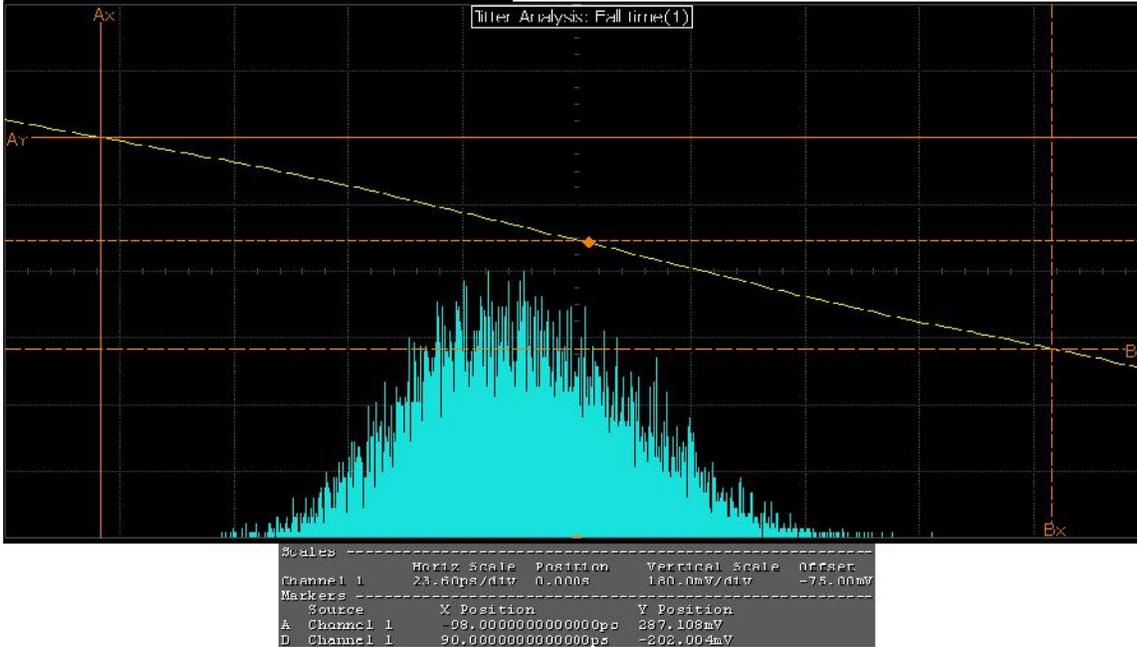
Test Limits: $\geq 75.000\text{ps}$ **Raw Clock Transition Time** 186.530ps

Result Details

Test Frequency(MHz) 296.966 **Upper Threshold(%)** 80.000 **Lower Threshold(%)** 20.000 **# Edges** 11.000000k

Trial 1

Trial 1: Raw Clock Transition Time



7-4: D0 - Rise Time

Reference: Test ID 7-4

Test Summary: Pass **Test Description:** | The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

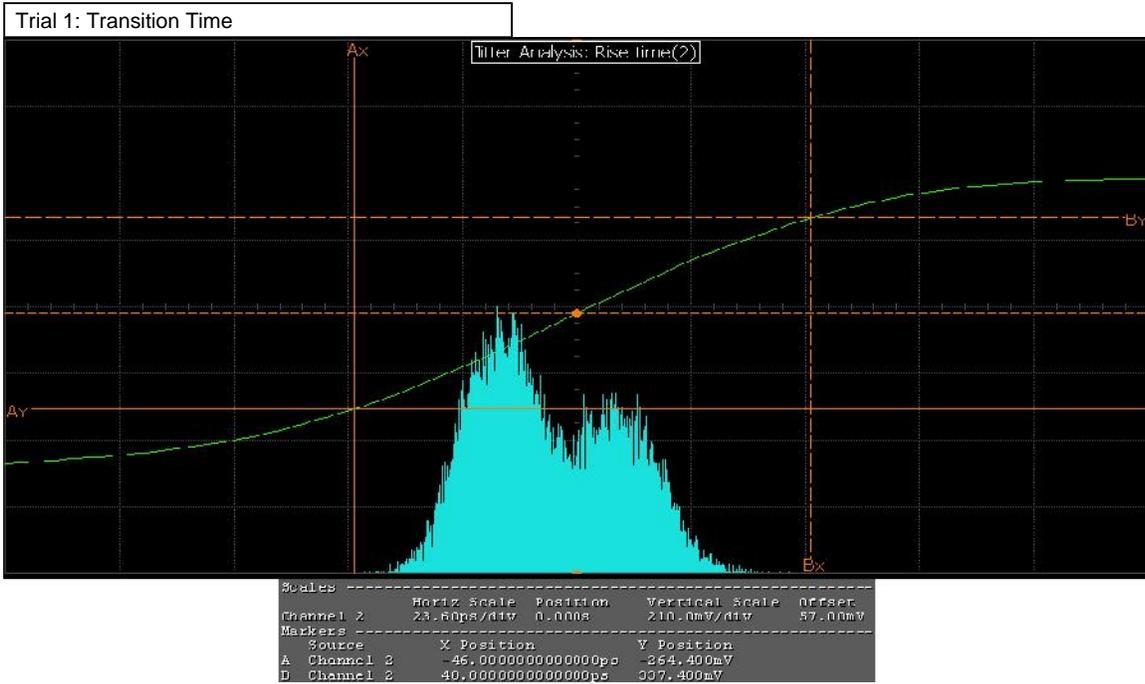
Test Limits: $\geq 75.000\text{ps}$ **Transition Time** 94.840ps

Result Details

Test Frequency(MHz) 296.966 **Data Lane A** D0 **Upper Threshold(%)** 80.000 **Lower Threshold(%)** 20.000

#Edge 25.168000k

Trial 1



✓ 7-4: D0 - Fall Time Reference: Test ID 7-4

Test Summary: Pass | Test Description: | The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

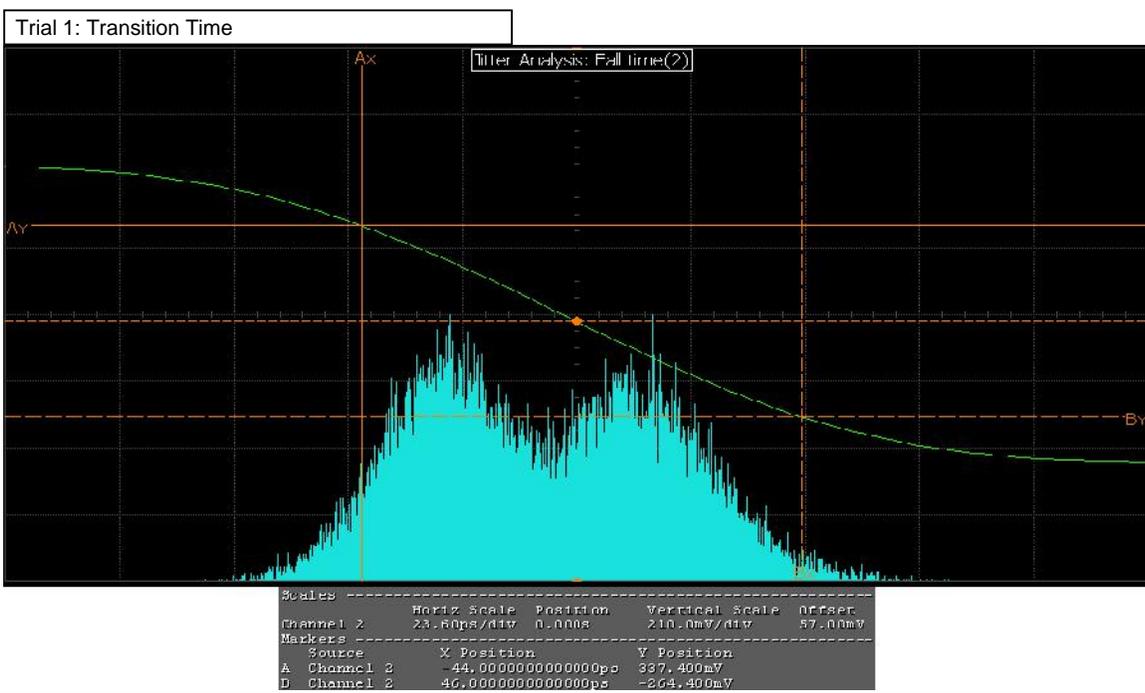
Test Limits: >= 75.000ps | **Transition Time** 93.580ps

Result Details

Test Frequency(MHz) 296.966 | **Data Lane A** D0 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000

#Edge 25.873000k

Trial 1



✓ 7-4: D1 - Rise Time

Reference: Test ID 7-4

Test Summary: Pass

Test Description: | The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: $\geq 75.000\text{ps}$

Transition Time 92.690ps

Result Details

Test Frequency(MHz) 296.966

Data Lane A D0

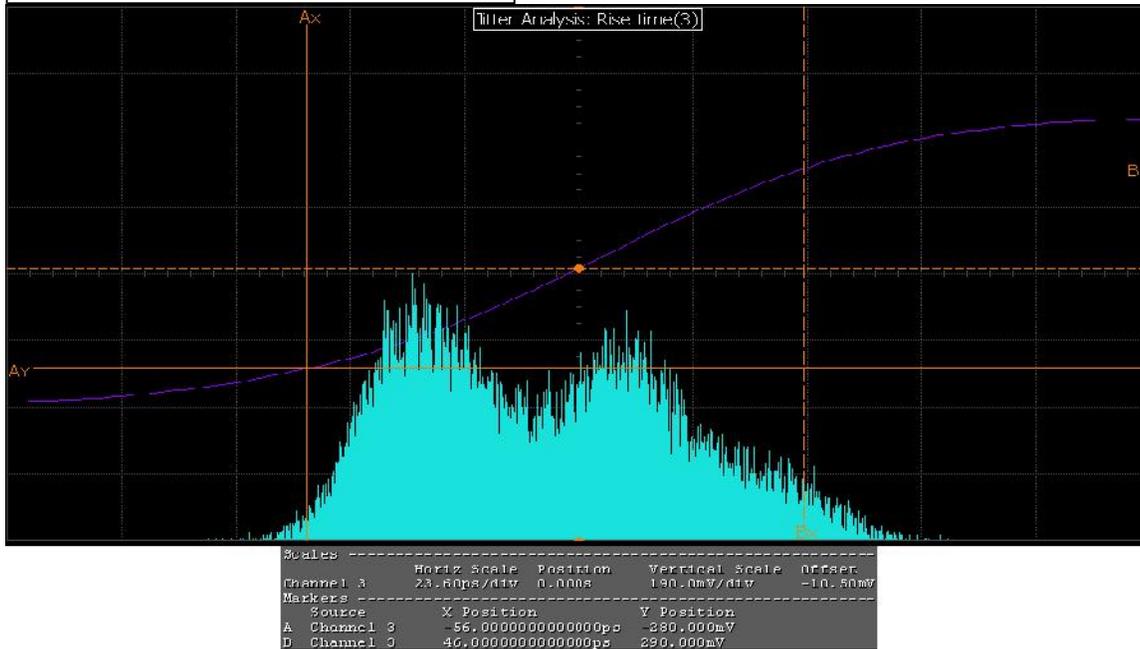
Upper Threshold(%) 80.000

Lower Threshold(%) 20.000

#Edge 25.852000k

Trial 1

Trial 1: Transition Time



✓ 7-4: D1 - Fall Time

Reference: Test ID 7-4

Test Summary: Pass

Test Description: | The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: $\geq 75.000\text{ps}$

Transition Time 90.320ps

Result Details

Test Frequency(MHz) 296.966

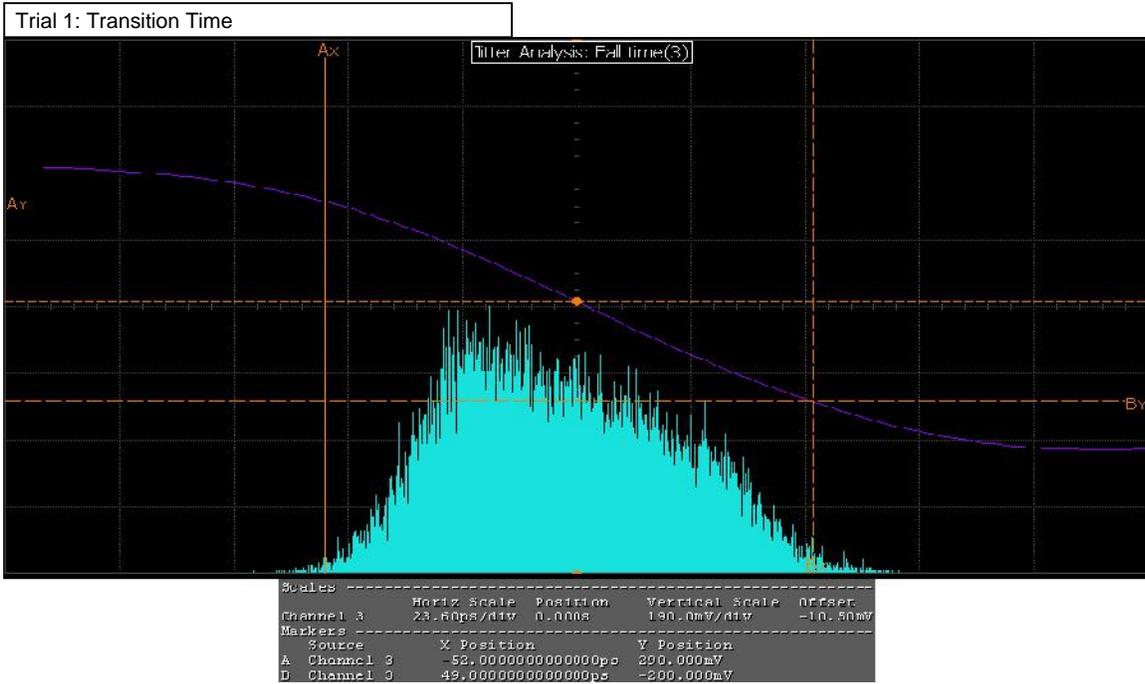
Data Lane A D0

Upper Threshold(%) 80.000

Lower Threshold(%) 20.000

#Edge 24.715000k

Trial 1



✓ 7-4: D2 - Rise Time Reference: Test ID 7-4

Test Summary: Pass | **Test Description:** | The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

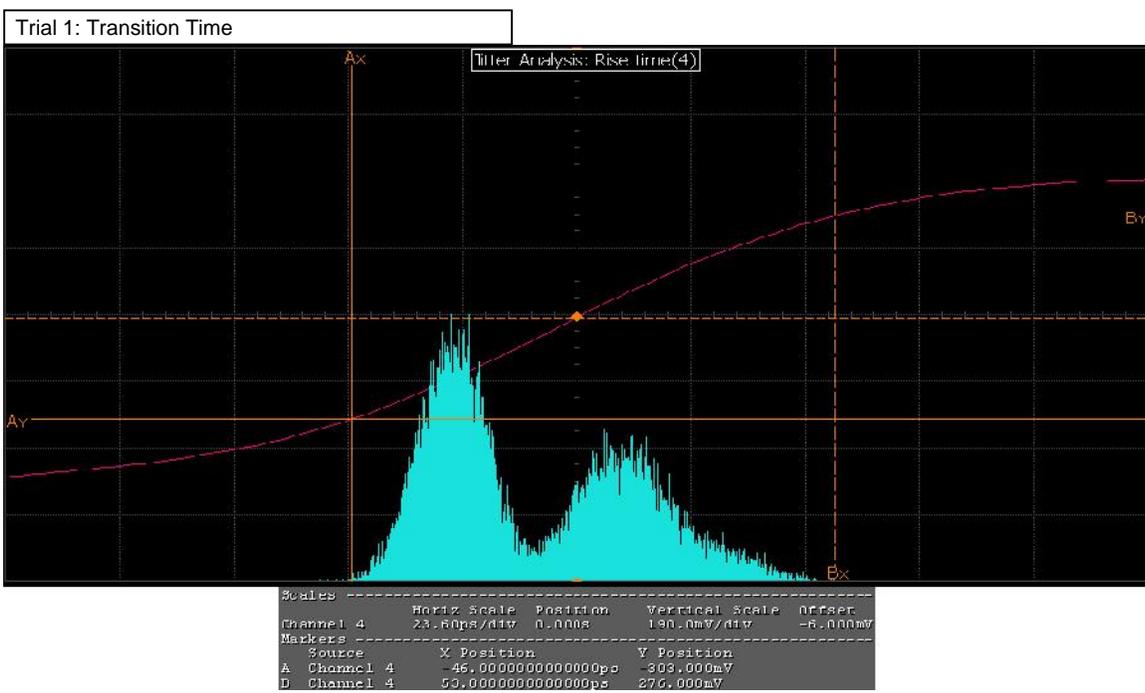
Test Limits: >= 75.000ps | **Transition Time** 99.130ps

Result Details

Test Frequency(MHz) 296.966 | **Data Lane A** D0 | **Upper Threshold(%)** 80.000 | **Lower Threshold(%)** 20.000

#Edge 24.813000k

Trial 1



✓ 7-4: D2 - Fall Time

Reference: Test ID 7-4

Test Summary: Pass

Test Description: | The transition time is defined as the time interval between the normalized 20% and 80% amplitude levels. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >= 75.000ps

Transition Time 93.070ps

Result Details

Test Frequency(MHz) 296.966

Data Lane A D0

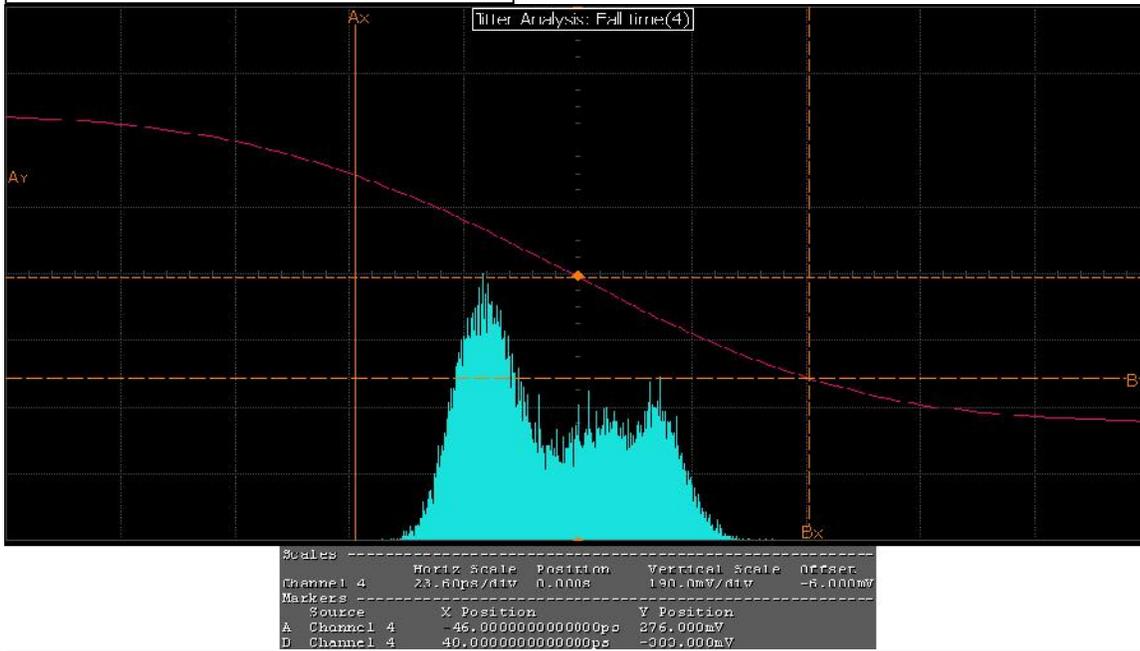
Upper Threshold(%) 80.000

Lower Threshold(%) 20.000

#Edge 24.787000k

Trial 1

Trial 1: Transition Time



7-8: Clock Duty Cycle(Minimum)

Reference: Test ID 7-8

Test Summary: Pass

Test Description: | 4 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: >=40%

Clock Duty Cycle Minimum 49.420

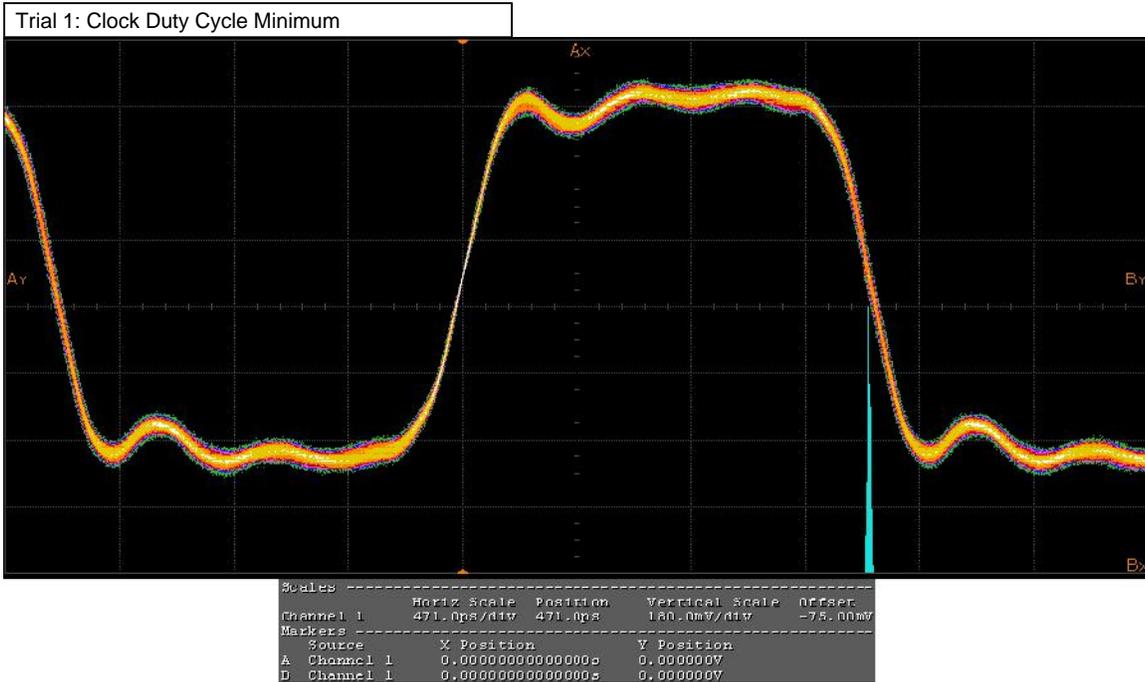
Result Details

Test Frequency(MHz) 296.966

Edges 10.000000k

TdutyMIN(ns) 1.664

Trial 1



✓ 7-8: Clock Duty Cycle(Maximum) Reference: Test ID 7-8

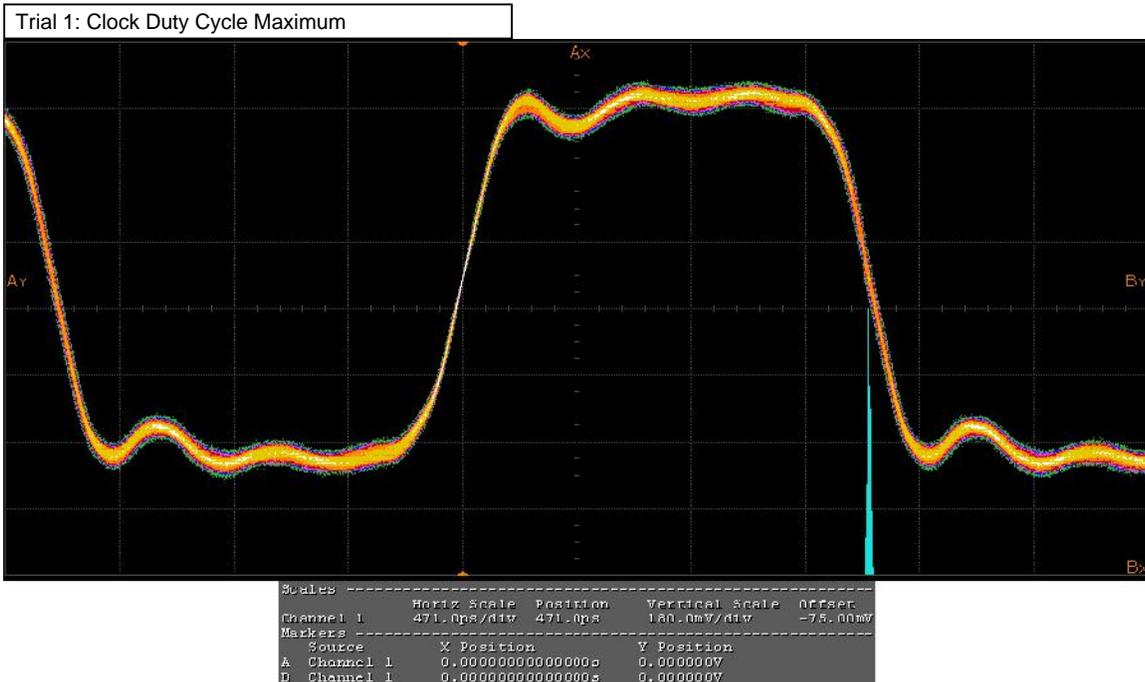
Test Summary: Pass | Test Description: | 4 Channels Connection Model: Clock duty cycle must be at least 40% and not more than 60%.The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: <=60% | Clock Duty Cycle Maximum 50.350

Result Details

Test Frequency(MHz) 296.966 | # Edges 10.000000k | TdutyMAX(ns) 1.696

Trial 1



✓ 7-6: Inter-Pair Skew - D0/D1

Reference: Test ID 7-6

Test Summary: Pass | **Test Description:** | Inter-pair skew must not exceed $0.20 \cdot T_{\text{pixel}}$. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: [-200mTpixel to 200mTpixel] | **Data - Data Inter-Pair Skew** 4mTpixel

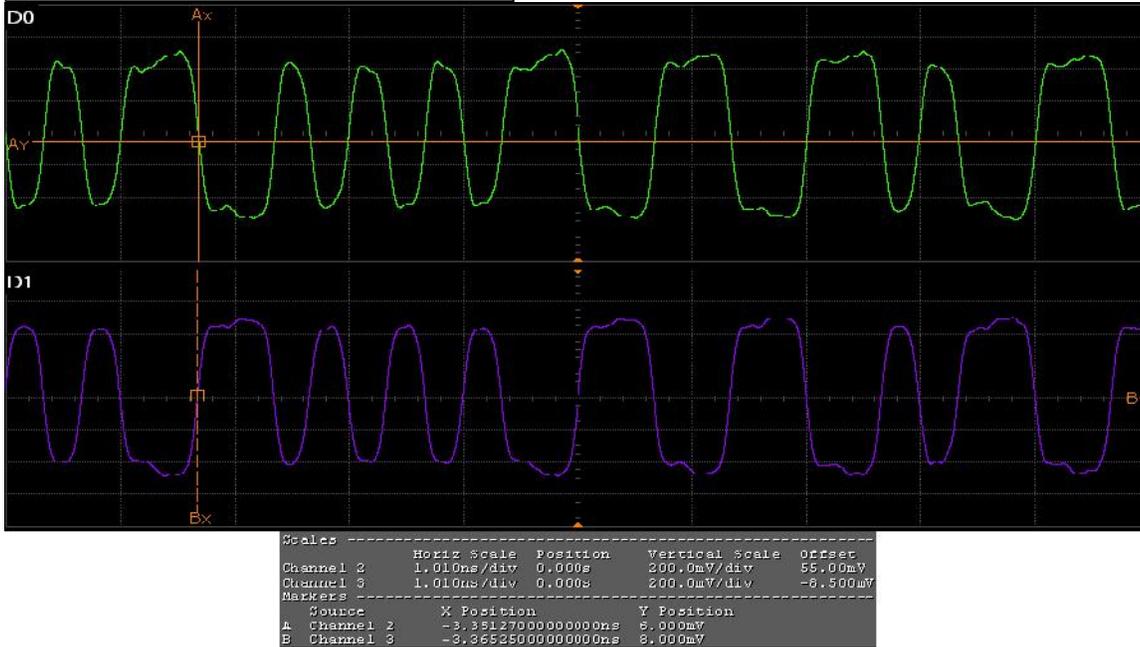
Result Details

Test Frequency(MHz) 296.966 | **Data Lane A** N/A | **Data Lane B** N/A | **Data - Data Inter-Pair Skew(ps)** 13.980

Triggered Pattern 20

Trial 1

Trial 1: Data - Data Inter-Pair Skew



✓ **7-6: Inter-Pair Skew - D0/D2**

Reference: Test ID 7-6

Test Summary: Pass | **Test Description:** | Inter-pair skew must not exceed $0.20 \cdot T_{\text{pixel}}$. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

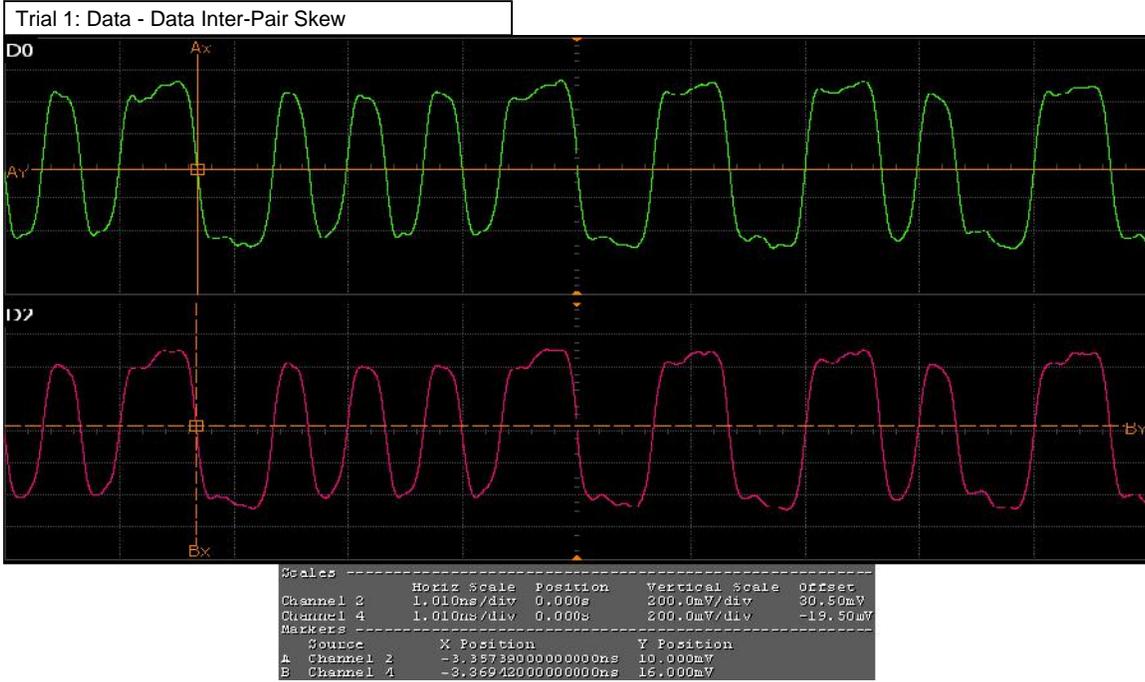
Test Limits: [-200mTpixel to 200mTpixel] | **Data - Data Inter-Pair Skew** 4mTpixel

Result Details

Test Frequency(MHz) 296.966 | **Data Lane A** N/A | **Data Lane B** N/A | **Data - Data Inter-Pair Skew(ps)** 12.030

Triggered Pattern 20

Trial 1



✓ 7-6: Inter-Pair Skew - D1/D2 Reference: Test ID 7-6

Test Summary: Pass | Test Description: Inter-pair skew must not exceed $0.20 \cdot T_{pixel}$. The Source shall meet the AC specifications in Table 4-13 across all operating conditions specified in Table 4-11. For compliance, the DUT should output the highest supported pixel clock frequency during the test.

Test Limits: [-200mTpixel to 200mTpixel] | Data - Data Inter-Pair Skew 2mTpixel

Result Details

Test Frequency(MHz) 296.966 | Data Lane A N/A | Data Lane B N/A | Data - Data Inter-Pair Skew(ps) 8.280

Triggered Pattern 20

Trial 1



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