

Product Name: ZX180CSI-HSPC FMC+ HSPC Vita 57.4 Connector Saver Debug Interposer

Product Description: The FPGA Connector Saver / Debug Interposer is a passive test and debug module designed for FMC+ (VITA 57.4) interfaces. It provides comprehensive access to power, control, management, configuration, clock, JTAG, and differential I/O signals while maintaining the electrical connectivity between the carrier and mezzanine modules.

The interposer features 14 rows × 40 pins (560 pins) and uses FMC+ High Serial Pin Count (HSPC) connectors, supporting both Terminal (SEAM, mezzanine side) and Socket (SEAF, carrier side) interfaces.

Designed for laboratory characterization, hardware debug, qualification, validation, and fault isolation, the module provides convenient probing and current-measurement access without requiring permanent modifications to the FPGA carrier or mezzanine board.

Full access to all **Power Supply** rails via onboard **10 mΩ Kelvin** current-measurement shunts. Access to all Control, Management , Configuration Sideband, differential clocks and clock-capable differential I/O signals including JTAG via onboard 0402 SMD shunts or test points.

The Vita57.4 assigned GND signals are inner connected with access at 3 onboard GND test points and the exposed copper on the TOP layer interfacing with test equipment, debug & development.

Fully compatible with **Vita 57.4 (FMC+ HSPC)** , and **backward compatible with Vita 57.1 (both HPC and LPC)** on Carrier and Mezzanine side.

Features:

- 1- 8-layer PCB stack-up optimized for high-speed signal integrity.
- 2- Power-rail monitoring through onboard precision 10 mΩ Kelvin current-sense shunts, with dedicated S+ and S- Kelvin sense terminals.
- 3- **Differential clock** access through dedicated test points for: REFCLK_M2C REFCLK_C2M SYNC_M2C SYNC_C2M differential pairs.
- 4- Control, management, configuration, and JTAG signal access through onboard 0402 SMD shunt footprints test points.
- 5- All **Clock-Capable** differential I/O signals are accessible via onboard 0402 SMD shunt footprints signals for the LA, HA, HB interfaces.
- 6- Access to signals from both the carrier and mezzanine sides for flexible debugging and characterization.
- 7- Improved signal integrity and crosstalk
- 8- Designed for laboratory characterization, debug, qualification, and fault isolation
- 9- Multiple dedicated GND test points connected directly to the internal ground planes & accessible via exposed top-layer copper.
- 10- 50 Ω controlled-impedance routing on all high-speed signals, with reference-plane control optimized for applications from DC to 10 GHz.
- 11- Designed for improved signal integrity and reduced crosstalk while maintaining the FMC/FMC+ signal path.
- 12- Designed for characterization, debugging, qualification, validation, and fault isolation.

Electrical: Insertion loss > -2dB @8GHz
Trace impedance: 50 Ω
Operating Temperature: -55°C to +125°C
Samtec Connector:
Onboard Connector: ASP-184329-1 14rows per 40
ASP-184330-01 14rows per 40
Mates with: Any Samtec SEAM & SEAF formfactor
Pitch: 0.020" (0.50mm) pin to pin pitch
Plating: 10μ" (0.25μm)
Shunt:
Package: Standard 0402 , 0805 SMD package
Power Resistors: **10 mΩ 10W 2511** SMD package

Compatibility: Primary standard: VITA 57.4 — FMC+
Backward compatibility: VITA 57.1 — FMC

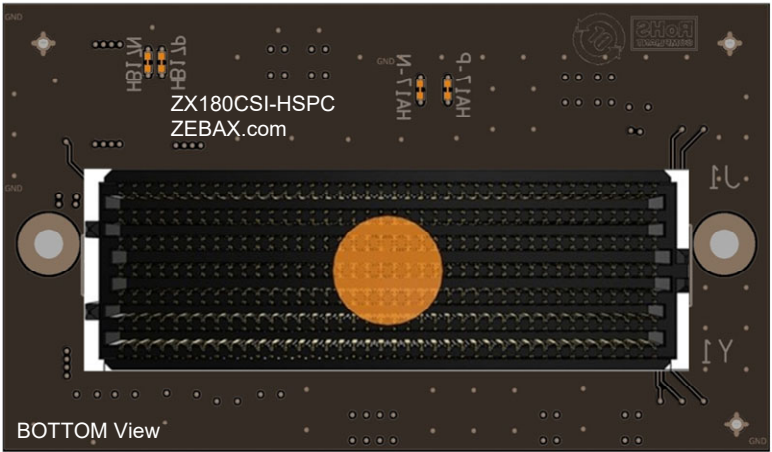
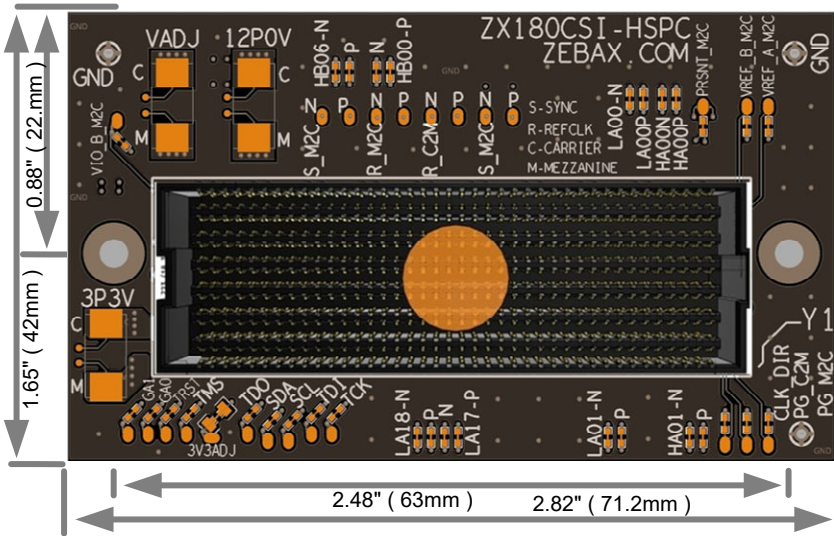
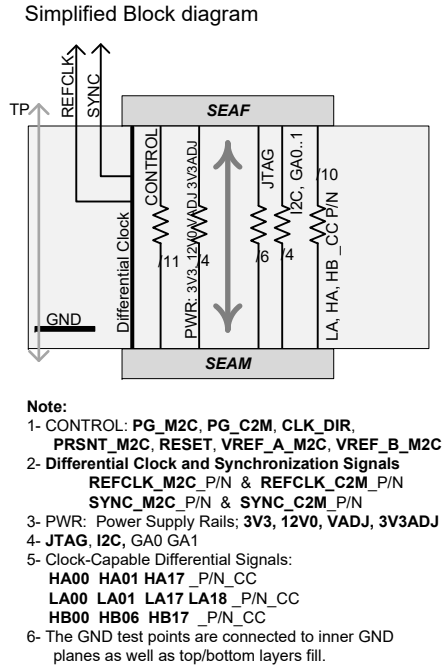
Application: FMC+ VITA 57.4 HPC LPC , Vita 57.4 FMC+ HSPC , daughter card Bringup, testing, emulation, Xilinx development interface testing daughter board to host, modular design evaluations Carrier-card ,Mezzanine-card bring-up System integration Power-rail characterization Current consumption measurement Clock integrity measurements JTAG debugging Reset and power-good monitoring Signal integrity characterization Fault isolation External signal injection Hardware emulation and validation Production qualification test and development automated validation automation

Access: The ZX180CSI-HSPC provides test points and SMD shunts for accessing the signals.
Refer to **Page 6** for details

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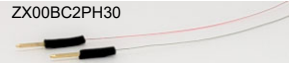
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Ordering Information:

Part number	Description
ZX180CSI-HSPC	Vita 57.4 Connector Saver Interposer test module
ZX00BC2PH30	30AWG Bare Copper wire to pin header wire assembly
ZX0002SRF4	High Frequency semi-rigid SMA to bare wire coax cable assembly

[ZX100ACC-SS site page](#) for ordering accessories, wire / cable assembly



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SPECIFIED DIMENSIONS ARE INCHES (MM). ROHS COMPLIANT		ASSEMBLY DRAWING
		ITEM: ZX180CSI-HSPC
DESCRIPTION: FMC+ HSPC VITA 57.4 Connector Saver Interposer test module.		
CHECKED:	DRAWN:	REVISION: 1.0
M. MARINA	SONYA	
		SHEET: 1 OF 6

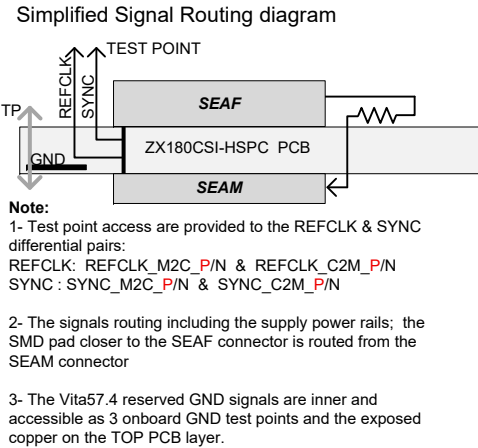
Product Name: Cont's ZX180CSI-HSPC FMC+ HSPC Vita 57.4 Connector Saver Debug Interposer

Mates with : The ZX180CSI-HSPC FMC+ HSPC VITA 57.4 Test Module is designed to mate with Samtec and Molex high-speed, high-density SEARAY HSPC connectors compliant with the VITA 57.4 FMC+ standard. The module is suitable for use with:

- Xilinx FPGA development systems, including daughter-board-to-host configurations.
- FMC+ High Serial Pin Count (HSPC) interfaces compliant with VITA 57.4.
- FMC+ carrier and mezzanine designs using compatible HSPC mating connectors.
- Compatible Vita 57.4-compliant HSPC connectors: ASP-188588-01 ASP-208521-01 ASP-184330-01 ASP-208571-01 ASP-184329-01 ASP-208573-01

ZX180CSI-HSPC FMC+ HSPC breakout adapter mates with the following Samtec SEARAY™ VITA 57.4 Connectors			
Samtec PN	VITA 57.4	Description	Mated Stack Height
ASP-188588-01	HSPC	Terminal	8.5mm
ASP-208521-01	HSPC	Terminal	8.5mm
ASP-184330-01	HSPC	Terminal	10mm
ASP-208571-01	HSPC	Terminal	10mm
ASP-184329-01	HSPC	Socket	Standard height
ASP-208573-01	HSPC	Socket	Standard height
Terminal : Also known as Male- It is usually located on Mezzanine card.			
Socket : Also known as Female, is usually located on Host or Carrier Side.			

Ground: The ZX180CSI-HSPC is an FMC+ passive Connector Saver / Debug Interposer providing access to VITA 57.4 interface signals. The VITA 57.4 assigned GND pins are not individually accessible; instead, they are connected to the internal GND planes and copper fills on the top and bottom PCB layers. Convenient ground access is provided through three onboard GND test points and exposed top-layer copper, enabling connection to test equipment for test and measurement, debugging, and development while maintaining a solid high-speed signal reference.

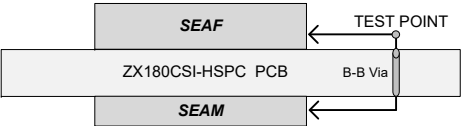


Signal Routing: The ZX180CSI-HSPC provides dedicated test points for the specified differential clock signals. All other accessible signals are routed through onboard SMD shunt footprints, which serve as bridges between the Carrier and Mezzanine cards.

As a general routing convention, the SMD shunt pad closest to the SEAF connector is connected to the Mezzanine side (SEAM), while the opposite pad is connected to the Carrier side (SEAF). This arrangement provides convenient access for signal probing, measurement, isolation, and debugging.

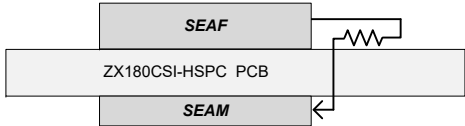
Isolated signal routing is implemented for the VIO_B_M2C and PRSNT_M2C signals because each signal has two assigned signal sources in the VITA 57.7 and VITA 57.1 standards. The ZX180CSI-HSPC routes each signal individually to its designated via through the associated 0402 SMD shunt. Refer to the VIO_B_M2C / PRSNT_M2C Routing Diagram for the detailed routing implementation.

Differential Clock Signal Routing diagram



Note:
1- Test point access are provided for the REFCLK & SYNC Differential Clock pairs:
REFCLK: REFCLK_M2C_P/N , REFCLK_C2M_P/N
SYNC : SYNC_M2C_P/N , SYNC_C2M_P/N
2-Internal PCB layers signal routing are connected at the test-point.

Simplified Signal Routing diagram



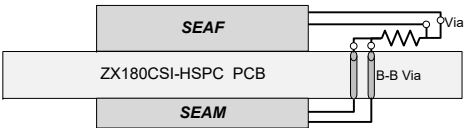
Note:
1- The signals routing including the supply power rails; the SMD pad closer to the SEAF connector is routed from the SEAM connector

Table 1- Accessible signals via test points or onboard SMD shunts

Signal Group	Signal	Direction	Access	TPP	C/M Isolation	Measurement Type
Management	PG_M2C	M→C	Shunt	402	Yes	Probe/inject
	PG_C2M	C→M	Shunt	402	Yes	Probe/inject
	CLK_DIR	C→M	Shunt	402	Yes	Probe/inject
	PRSNT_M2C	M→C	Shunt	402	Yes	Probe/inject
Sideband	VREF_A_M2C	M→C	Shunt	402	Yes	Probe/inject
	VREF_B_M2C	M→C	Shunt	402	Yes	Probe/inject
Power rails	12V0	C↔M	Current shunt	2510	Yes	Voltage / Current
	3V3	C↔M	Current shunt	2510	Yes	Voltage / Current
	VADJ	C↔M	Current shunt	2510	Yes	Voltage / Current
	3V3VADJ	C↔M	Current shunt	0805 / 0402	Yes	Voltage / Current
Differential Clocks	REFCLK_M2C_P/N	M→C	TP	—	No	Scope
	REFCLK_C2M_P/N	C→M	TP	—	No	Scope
	SYNC_M2C_P/N	M→C	TP	—	No	Scope
	SYNC_C2M_P/N	C→M	TP	—	No	Scope
I2C	I2C - SDA	bidirectional	Shunt	402	Yes	Probe/inject
	I2C - SCL	C→M (typically)	Shunt	402	Yes	Probe/inject
Configuration	GA0	M→C	Shunt	402	Yes	Probe/inject
	GA1	M→C	Shunt	402	Yes	Probe/inject
JTAG	TCK	C→M	Shunt	402	Yes	Probe/inject
	TMS	C→M	Shunt	402	Yes	Probe/inject
	TDI	C→M	Shunt	402	Yes	Probe/inject
	TDO	M→C	Shunt	402	Yes	Probe/inject
	TRST_L	C→M	Shunt	402	Yes	Probe/inject
Clock-Capable Differential I/O	LA00_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	LA01_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	LA17_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	LA18_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	HA00_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	HA01_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	HA17_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	HB00_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	HB06_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject
	HB17_P/N_CC	Bidirectional	Shunt	402	Yes	Probe/inject

TPP : Test Point Package
C/M Isolation : Removing the shunt's inner connecting trace, isolate Carrier / Mezzanine signal path.

VIO_B_M2C and PRSNT_M2C Signal Routing



Note:
1- Isolated signal routing is implemented for the VIO_B_M2C and PRSNT_M2C signals since each signal has two assigned signal sources. The ZX180CSI-HSPC routes each signal individually to its designated via through the associated 0402 SMD shunt.

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ASSEMBLY DRAWING
ITEM: ZX180CSI-HSPC

DESCRIPTION: FMC+ HSPC VITA 57.4 Connector Saver Interposer test module.

CHECKED: M. MARINA

DRAWN: SONYA

REVISION: 1.0
SHEET: 2 OF 6

Product Name: Cont’s ZX180CSI-HSPC FMC+ HSPC Vita 57.4 Connector Saver Debug Interposer

Power-Rail Measurement: Selected power rails on the ZX180CSMPS-HSPC are routed through precision 10 mΩ, 4-terminal SMD current-sense shunts. Each shunt provides dedicated S+ and S– Kelvin sense connections for accurate current measurement.

Signal Group	Signal	Direction	Access	TPP	C/M Isolation	Measurement Type
Power rails	12V0	C↔M	Current shunt	2510	Yes	Voltage / Current
	3V3	C↔M	Current shunt	2510	Yes	Voltage / Current
	VADJ	C↔M	Current shunt	2510	Yes	Voltage / Current
	3V3VADJ	C↔M	Current shunt	0805 / 0402	Yes	Voltage / Current

Supported Power Rails: The supported power rails are: VADJ 12V0 3V3 3V3ADJ

Each power rail provides clearly identified Carrier-side (C) and Mezzanine-side (M) connections. PCB silkscreen markings identify the routing direction:

C — Carrier side
M — Mezzanine side

These markings allow the user to quickly determine the location and direction of the measured power path relative to the Carrier and Mezzanine interfaces.

Current and Voltage Measurement

The voltage developed across each 10 mΩ current-sense shunt can be measured using the dedicated Kelvin S+ and S– connections.

The load current is calculated as: I = VSHUNT / 0.010 Ω

Examples: 10 mV across the shunt = 1 A
50 mV across the shunt = 5 A
100 mV across the shunt = 10 A

External Power Injection and Power Analysis: In addition to voltage and current measurement, the shunt architecture provides the option to remove the current-sense shunt and externally power either the Carrier or Mezzanine card.

- This configuration enables the user to connect an external laboratory power supply directly into the desired power path and perform real-time power-integrity characterization, including analysis of:
- Power-supply noise
 - Voltage droop and transient response
 - Frequency-domain characteristics
 - Nyquist analysis
 - Bode plots
 - Other power-integrity measurements as required

This capability makes the interposer useful for detailed power characterization, debugging, qualification, and fault isolation.

3V3ADJ Debug Access: The 3V3ADJ power rail incorporates a debug architecture similar to the VADJ, 12V0, and 3V3 rails. Both 0805 and 0402 SMD shunt footprints are provided to support measurement, configuration, and power-path access.

Unlike the VADJ, 12V0, and 3V3 rails, the 3V3ADJ implementation does not include dedicated S+ / S– Kelvin sense connections.

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FMC+ HSPC VITA 57.4 Connector Saver Interposer test module.

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DRAWN: SONYA

REVISSION: 1.0

SHEET: 3 OF 6

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Product Name: Cont’s ZX180CSI-HSPC FMC+ HSPC Vita 57.4 Connector Saver Debug Interposer

Clock-Capable Differential Signal : Selected **clock-capable differential signals** are routed through onboard **0402 SMD shunt footprints**, providing convenient access for probing, signal characterization, isolation, and controlled test configurations.

Each selected differential signal is routed through an individual 0402 shunt, with the **Mezzanine-side (SEAM)** and **Carrier-side (SEAF)** connections routed separately to the two shunt pads. Refer to the “**Signal Routing**” section for the applicable routing convention and pad assignments.

For ease of identification, the PCB silkscreen provides abbreviated labeling for the clock-capable differential signal groups. Depending on available board space, labels may use the corresponding **CC (Clock-Capable)** designation. For example:

LA00_P may be labeled for **LA00_CC_P**
LA00_N may be labeled for **LA00_CC_N**
Similar labeling conventions are used for other applicable **LA, HA, and HB clock-capable differential signals**.

This arrangement provides flexible access to selected high-speed differential signals while maintaining a controlled and organized signal path between the Carrier and Mezzanine interfaces.

Differential Clock and Synchronization Signals : The **Differential Clock and Synchronization signals** are routed to dedicated test points located on the top side of the module, providing convenient access for probing, measurement, characterization, and debugging.

Four differential clock/synchronization pairs are provided, with dedicated **P/N test points** for each differential pair.

In this document, “**P**” designates the **positive (non-inverting)** signal, while “**N**” designates the **negative (inverting)** signal of a differential pair. For example, **REFCLK_M2C_P/N** refers collectively to the two signals **REFCLK_M2C_P** and **REFCLK_M2C_N**.

Signal Routing: The differential clock and synchronization signals are routed through **PCB Layers 3 and 5** and brought together at their respective designated test points. This routing architecture provides controlled signal paths while maintaining convenient top-side access for laboratory instrumentation. Refer to the “**Signal Routing**” section for detailed routing information and diagrams.

Clock and Synchronization Signal Identification: The table below lists the available differential clock and synchronization signals along with their corresponding **PCB silkscreen designations**. Each differential clock pair has individually routed positive (P) and negative (N) test points, allowing each side of the differential signal to be probed independently.

The PCB uses abbreviated silkscreen labels, with P and N identified separately for clear signal-pair identification.

Signal Group	Signal	Silkscreen	Direction	Access	TPP	C/M Isolation	Description
Differential Clocks	REFCLK_M2C_P/N	R_M2C P/N	M→C	TP	SMD	No	Differential reference clock pair, Mezzanine-to-Carrier
	REFCLK_C2M_P/N	R_C2M P/N	C→M	TP	SMD	No	Differential reference clock pair, Carrier-to-Mezzanine
	SYNC_M2C_P/N	S_M2C P/N	M→C	TP	SMD	No	Differential synchronization clock pair, Mezzanine-to-Carrier
	SYNC_C2M_P/N	S_C2M P/N	C→M	TP	SMD	No	Differential synchronization clock pair, Carrier-to-Mezzanine

Configuration, Management, and Sideband Test Access: Table 3 lists the configuration, management, and sideband signals accessible through the ZX180CSI-HSPC module. Each selected signal is routed through an individual **0402 SMD shunt footprint**, providing convenient access for probing, characterization, isolation, and debugging. The two sides of each shunt are routed separately to the Mezzanine (SEAM) and Carrier (SEAF) connectors. Refer to the “**Signal Routing**” section for detailed routing information and shunt pad assignments.

Table 2- Clock -Capable Differential Signals

Signal Group	Signal	Direction	Access	TPP
Clock-Capable Differential I/O	LA00_P/N_CC	Bidirectional	Shunt	402
	LA01_P/N_CC	Bidirectional	Shunt	402
	LA17_P/N_CC	Bidirectional	Shunt	402
	LA18_P/N_CC	Bidirectional	Shunt	402
	HA00_P/N_CC	Bidirectional	Shunt	402
	HA01_P/N_CC	Bidirectional	Shunt	402
	HA17_P/N_CC	Bidirectional	Shunt	402
	HB00_P/N_CC	Bidirectional	Shunt	402
	HB06_P/N_CC	Bidirectional	Shunt	402
	HB17_P/N_CC	Bidirectional	Shunt	402

TPP : Test Point Package

Table 3- Configuration management and Sideband

Signal Group	Signal	Direction	Access	TPP	C/M Isolation	Measurement Type
Management	PG_M2C	M→C	Shunt	402	Yes	Probe/inject
	PG_C2M	C→M	Shunt	402	Yes	Probe/inject
	CLK_DIR	C→M	Shunt	402	Yes	Probe/inject
	PRSNT_M2C	M→C	Shunt	402	Yes	Probe/inject
Sideband	VREF_A_M2C	M→C	Shunt	402	Yes	Probe/inject
	VREF_B_M2C	M→C	Shunt	402	Yes	Probe/inject
I2C	I2C - SDA	bidirectional	Shunt	402	Yes	Probe/inject
	I2C - SCL	C→M (typically)	Shunt	402	Yes	Probe/inject
Configuration	GA0	M→C	Shunt	402	Yes	Probe/inject
	GA1	M→C	Shunt	402	Yes	Probe/inject
JTAG	TCK	C→M	Shunt	402	Yes	Probe/inject
	TMS	C→M	Shunt	402	Yes	Probe/inject
	TDI	C→M	Shunt	402	Yes	Probe/inject
	TDO	M→C	Shunt	402	Yes	Probe/inject
	TRST_L	C→M	Shunt	402	Yes	Probe/inject

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ASSEMBLY DRAWING
ITEM: ZX180CSI-HSPC

DESCRIPTION:

FMC+ HSPC VITA 57.4 Connector Saver
Interposer test module.

CHECKED:
M. MARINA

DRAWN:
SONYA

REVISSION: 1.0
SHEET: 4 OF 6

Product Name: Cont’s ZX180CSI-HSPC FMC+ HSPC Vita 57.4 Connector Saver Debug Interposer

Access map: Table 4 provides the VITA 57.4 signal access map with corresponding VITA 57.1 HPC and LPC signal mappings.

The ZX180CSI-HSPC provides access to the full set of VITA 57.4 FMC+ HSPC signals and supports interfacing with compatible VITA 57.1 FMC connector configurations, including both HPC (High Pin Count) 10 × 40 and LPC (Low Pin Count) 4 × 40 interfaces.

Interface Definitions:

- FMC LPC — VITA 57.1 Low Pin Count (LPC), 4 × 40-pin grid.
- FMC HPC — VITA 57.1 High Pin Count (HPC), 10 × 40-pin grid.
- FMC+ HSPC — VITA 57.4 High Serial Pin Count (HSPC) FMC+ interface.

The access map identifies the corresponding signal locations and compatibility across these FMC and FMC+ interface configurations.

Compatibility Cross Reference: The table below provides a cross-reference of the mechanical and electrical compatibility between the VITA 57.1 FMC HPC/LPC and VITA 57.4 FMC+ HSPC connector interfaces.

VITA 57.4 FMC+ maintains backward compatibility with VITA 57.1 FMC mezzanine cards. An HSPC carrier connector can accept an FMC HPC or LPC mezzanine connector; however, signals that are not present on the legacy HPC/LPC interface are treated as no-connects.

Table 5- Compatibility cross reference

Source	FMC LPC	FMC HPC	FMC+ HSPC
FMC LPC	Yes	Yes ¹	Yes ¹
FMC HPC	Yes ¹	Yes	Yes ¹
FMC+ HSPC	No	No	Yes

Note: 1- Mechanically compatible. The low est FMC signals mapping w ill be available.

Table 4- Vita 57.7, Vits 57.1 signal mapping

Vita 57.4 (FMC+ - HSPC) 14 x 40														
Vita 57.1 (FMC - HPC) 10x40														
Vita 57.1 (FMC - LPC) 4x40														
Pin	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_P	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17-P-CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17-N-CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00-P-CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00-N-CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06-P-CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06-N-CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10-P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TD0	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10-N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14-P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14-N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	DP5_C2M_P	GND	DP19_M2C_P	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND
FMC LPC					X	X			X	X				
FMC HPC			X	X	X	X	X	X	X	X	X	X		
FMC+ HSPC	X	X	X	X	X	X	X	X	X	X	X	X	X	X

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SPECIFIED DIMENSIONS ARE INCHES (MM). ROHS COMPLIANT		ASSEMBLY DRAWING	
		ITEM: ZX180CSI-HSPC	
DESCRIPTION:		FMC+ HSPC VITA 57.4 Connector Saver Interposer test module.	
CHECKED: M. MARINA		DRAWN: SONYA	
		REVISION: 1.0	
		SHEET: 5 OF 6	

Product Name: Cont's ZX180CSI-HSPC FMC+ HSPC Vita 57.4 Connector Saver Debug Interposer

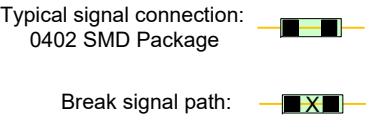
Test Points and SMD Shunts: The ZX180CSI-HSPC provides test points and SMD shunts for accessing designated signals. The shunts serve as bridges between the Carrier and Mezzanine cards while providing convenient interfaces for external test and measurement equipment.

The 0402 SMD shunts are implemented as PCB-designed 0402 footprints, with the two landing pads connected by an inner PCB trace. This connecting trace can be physically removed (cut) to isolate the signal, enabling independent test and measurement from either the Carrier or Mezzanine side.

After isolation, the 0402 footprint can accommodate discrete components such as current-limiting or termination resistors, AC-coupling capacitors, ferrite beads, or other passive components. These components can be used to modify the signal path for characterization, filtering, termination, and other test purposes.

The isolated nodes also allow external test equipment or circuitry to be connected for controlled signal injection, subsystem emulation, fault isolation, validation, characterization, and debugging.

For high-speed signals, test connections and component placement should minimize additional parasitic capacitance, inductance, stubs, and impedance discontinuities to avoid adversely affecting signal integrity.



Accessories: The following accessories complement the module and provide convenient interfaces for testing, characterization, and performance evaluation.

ZX00BC2PH30 – 30 AWG Bare Copper Wire-to-Pin Header Assembly: A flexible wire assembly that can be easily soldered to designated pads on the ZX180CSI-HSPC to provide convenient access for oscilloscope probes and other test equipment.



ZX0002SRF4 – High-Frequency SMA-to-Bare-Wire Semi-Rigid Coaxial Cable Assembly: A semi-rigid coaxial cable with an exposed copper outer conductor that can be directly soldered to designated pads on the module. With an insertion loss of less than 0.5 dB, this assembly provides a low-loss connection suitable for high-frequency signal characterization and performance qualification.



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		SHEET: 6 OF 6

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