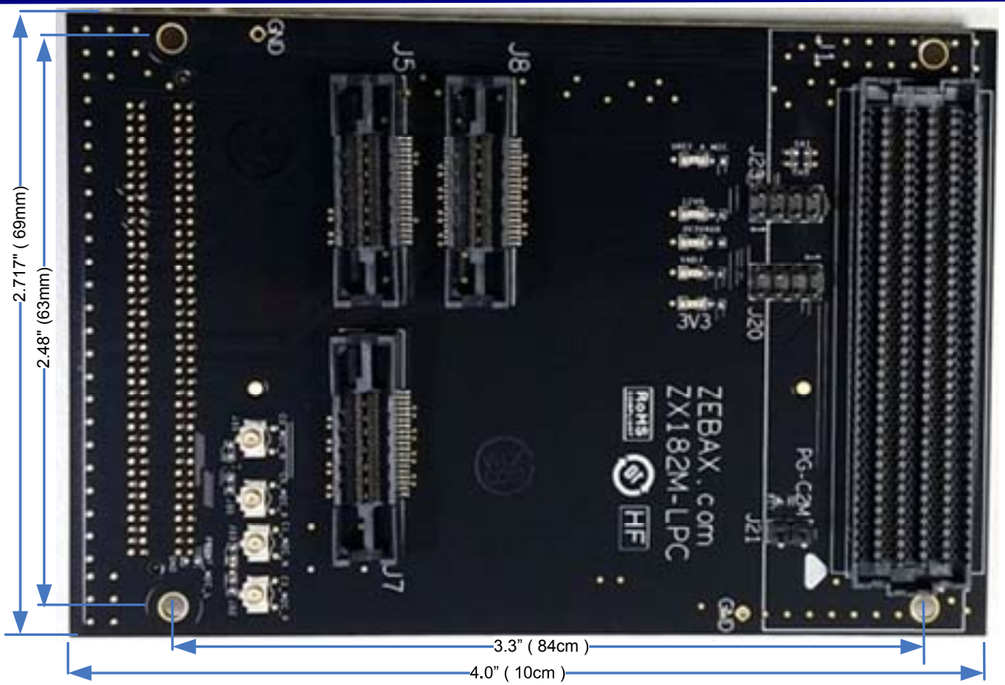
Product Name: **ZX182M-LPC FMC Vita 57.1 test mezzanine card module designed to work with Keysight Tektronix Mictor connector Logic Analyzer or any flying probe.**
Keysight (Agilent) - Mictor probes : E5346A E5380A E5381A E5382A
Tektronix – Mictor Probe P6434

Product Description: FPGA Mezzanine card , FMC , passive breakout adapter, meeting VITA 57.1 standard bus interfacing with Keysight and Tektronix Mictor or flying leads differential / single ended probes. Includes 4 rows x 40 pins, totaling **160** pins, Low Pin Count , LPC , rows 3, 4, 7, 8 (C, D, G, H rows) are available pins Low Pin Count, LPC. Onboard both CC (Carrier Card - Host) and MC (Mezzanine Card) connectors.

ZX182M-LPC is offered in LPC connector configuration, see ordering information

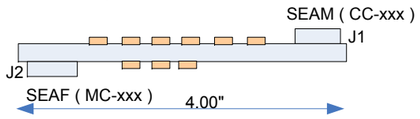
Fully compatible with 4 rows x 40 pins single ended or differential pairs design configuration
- **All** signals are accessible via designated probe's connector, IPEX, Header, and 0402 SMD package.
- All Clocks are accessible via IPEX-37 connectors
- JTAG signals accessible via 2x4 pin header
- All Power Supply signals accessible via 2x4 pin headers with on-board LEDs indicators.
- Improved signal integrity and crosstalk with **10 layers PCB** with each layers guarded by GROUND plane.
- Designed for **50Ω** single ended and **100Ω** differential trace impedance exceeding VITA 57.1 standard.
- DC to 10GHz bandwidth applications

GND test point for easy access as well as applying external ground reference



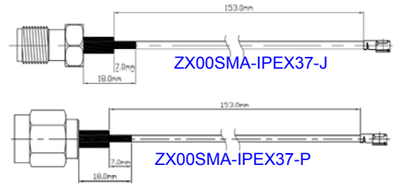
ZX182M-LPC Block diagram, See Page 2, 3

ZX182M-LPC , Passive FMC VITAL 57.1
breakout adapter – test board



CC: Carrier Card typically located on Host
MC: Mezzanine Card, typically located on Mezzanine Card
SEAF: SEARRAY Female connector
SEAM: SEARRAY Plug (Male) connector

Probe connector, headers, IPEX-37 access points



ZX182M-LPC-X Package includes:

Part number	Quantity	Description
ZX182M-LPC-X	1	FMC Mezzanine Module
ZX00SMA-IPEX37-X	4	SMA to IPEX-37 cable assembly , Note 1
ZX104LN-RA	0	Mictor breakout adapter
ZX104x	0	Mictor Breakout adapter

Notes:
1- Used for measuring or supplying external Clocks, see ordering information.

Application: FMC VITA 57.1 daughter card Bringup, testing, emulation, Xilinx development Virtex 6 Virtex 7 interface testing daughter board to host, modular design evaluations

Access: 2x4 header, SMD 0402 Package footprint as well as Mictor Probe receptacle P6834, P68xx E5346A E5380A E5381A E5382A connector interface

Pitch: 1.27mm (0.05") High Speed connector

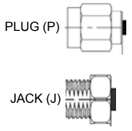
Mates with : Xilinx FPGA development systems Virtex 6 Virtex 7 connecting daughter board to Host
Any and all FMC VITA 57.1 compliant design CC-LPC-xxx MC-LPC-xxx
where xxx is 10L, 10, 8.5L 8.5 Samtec Molex
HI-SPEED HI-DENSITY SEARRAY design connectors.
SEAM SADL SEAMP SEAR SEAMI SEAC FMC LCP
SEAF-040-08.0-L-10-2-A SEAF-040-08-L-10-2-A
SEAFP-40 SEAMP-040 SEAMI-040 SEAM-040
All listed Samtec Molex FMC connectors listed, table below:

ZX182xLPC FMC breakout adapter mates with the following Samtec Molex CC / MC SEARAY™ VITA 57.1 Connectors

Molex PN	Samtec PN	VITA PN	Description	Mated Stack Height
45971-4307	ASP-127796-01*	CC-LPC-10L	female	
45971-4305	ASP-134603-01	CC-LPC-10	female	
45970-4107	ASP-134605-01*	MC-LPC-8.5L	male	8.5 mm
45970-4105	ASP-134606-01	MC-LPC-8.5	male	8.5 mm
45970-4307	ASP-127797-01	MC-LPC-10L	male	10 mm
45970-4305	ASP-134604-01	MC-LPC-10	male	10 mm

ZX104x (from Zebax) products complement ZX182M providing flying leads interface to any scope or Logic Analyzer.

Ordering INFO:
Part Number
ZX182M-LPC-X options
J : SMA Jack (Standard)
P: SMA Plug connector



Note
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SPECIFIED DIMENSIONS ARE INCHES (MM).
ROHS COMPLIANT

ASSEMBLY DRAWING

ITEM: ZX182M-LPC-X

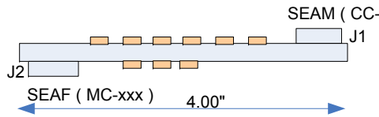
DESCRIPTION: **FMC VITA 57.1 LPC test board Agilent Tektronix Mictor or Flying Leads probe passive mezzanine**

CHECKED: M. MARINA
DRAWN: SLAVIK
REVISSION: 1.0
SHEET: 1 OF 3

Product Name: **ZX182M-LPC FMC Vita 57.1 Keysight Tektronix Mictor connector probe test board - breakout adapter passive FPGA Mezzanine Card**

Keysight (Agilent) - Mictor probes : E5346A E5380A E5381A E5382A
Tektronix – Mictor Probe P6434

ZX182M-LPC, Passive FMC VITAL 57.1 breakout adapter – test board



CC: Carrier Card typically located on Host
MC: Mezzanine Card, typically located on Mezzanine Card
SEAF: SEARRAY Female connector
SEAM: SEARRAY Plug (Male) connector

Probe connector, headers, IPEX-37 access points

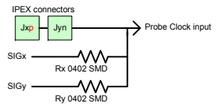
Typical SS signal connection using 0402 SMD Package

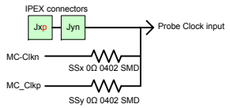
Break signal path:

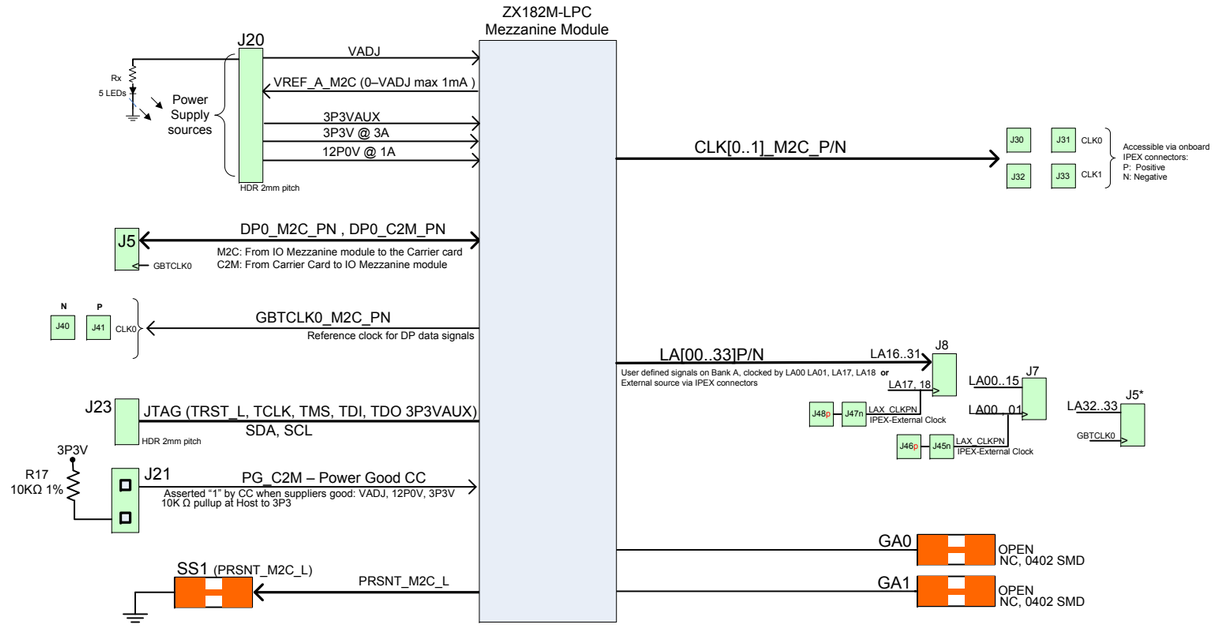
Clock routing technique

Probe clocks are routed using IPEX connectors for use with external clock sources as well as optional resistor stuffing as exhibited below. Jxp, Jxn are IPEX positive and negative IPEX connectors. The Rx, Ry (0402 SMD package) are not stuffed as default. SIGx, SIGy are defined signals reserved as probe clock option, if available. Please see Probe signal assignment table for assigned IPEX and availability of SIGx, SIGy per designed probe access.

MC clock source routing to probes are accessible at IPEX connectors. SS (0402 SMD package) can be used to disconnect MC from providing the Clock or install appropriate filtering, if applicable.







Note:
1- MC Mezzanine Card - **CC** Carrier Card (Host)
2- All Clocks are accessible via onboard IPEX connectors
3- IPEX Jxxp is positive terminal, Jxxn is negative terminal of the external clock source.
4- J5* - J5 is shared connector supporting DP0_M2C_PN, DP0_C2M_PN and LA32 and LA33 signal pairs.

Note

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SPECIFIED DIMENSIONS ARE INCHES (MM). ROHS COMPLIANT	ASSEMBLY DRAWING
	ITEM: ZX182M-LPC
DESCRIPTION:	FMC VITA 57.1 LPC test board Agilent Tektronix Mictor or Flying Leads probe passive mezzanine
CHECKED: M. MARINA	DRAWN: SLAVIK
REVISSION: 1.0	SHEET: 2 OF 3

Probe signal map: Below are signal and clock mapping for the designated probe connectors

J5					
Assigned	Pin	Signal	Signal	Pin	Assigned
NC	1	NC	NC	2	NC
NC	3	NC	NC	4	NC
NC	5	CLK0	CLK1	6	NC
	7	D15	D15	8	GBTCLK0-M2C-N J40 - SS18
	9	D14	D14	10	GBTCLK0-M2C-P J41 - SS19
	11	D13	D13	12	
	13	D12	D12	14	
	15	D11	D11	16	
	17	D10	D10	18	
	19	D9	D9	20	
	21	D8	D8	22	
	23	D7	D7	24	
	25	D6	D6	26	
LA33-N	27	D5	D5	28	LA32-N
LA33-P	29	D4	D4	30	LA32-P
	31	D3	D3	32	
	33	D2	D2	34	
DP0-C2M-N	35	D1	D1	36	
DP0-C2M-P	37	D0	D0	38	
GND(Center Tab)					

* CC and MC signals connected via SS18 & SS19. Signal measurement (or external stimulus) may be done via IPEX J40 and IPEX 41 connectors

J20			
Assigned	Pin	Pin	Assigned
	1	2	3P3
VREF-A-M2C	3	4	VADJ
	5	6	3P3VAUX
GND	7	8	12P0V

J23			
Assigned	Pin	Pin	Assigned
TDI	1	2	TDO
3P3VAUX	3	4	TCK
I2C-SCL	5	6	TRST-L
I2C-SDA	7	8	TMS

J21			
Assigned	Pin	Pin	Assigned
PG-C2M	1	2	3P3*

* 10 K Ω (R17) pullup resistor to 3P3 supply rail

Vita57.1 Power Supply rails			
Voltage supply	Voltage	Max. Current HPC (LPC)	Description
VADJ	0- 3.3V	4A (2A)	Adjustable supply voltage from CC to the IO MC module.
VREF-A-M2C	0 - VADJ	1mA*	Reference voltage used by the bank A data pins, LAxx, HAxx. No Connect if Bank A reference voltage is not required.
3P3VAUX	3.3V	20mA*	Auxiliary power supply from CC to the IO MC module.
3P3	3.3V	3A	Power supply from CC to the IO MC module.
12P0V	12.0V	1A	Power supply from CC to the IO MC module.

NA: Not available for LPC connector **CC:** Carrier Card (Host) **MC:** Mezzanine Card

* Due to supply rail's max. current limitation, the onboard LED indicator is populated but the current limiting resistor is NOT populated.

NOTES:

+ IPEX connector access to the probe connector. The SSxx (0402 SMD package) enables MC Signal source. The SSxx Can be replaced by bead, ac coupling cap or filter.

++ Probe clock can be supplied from listed source, IPEX connector (if Jxx is listed) (X - Rx) and (Y-Ry) where X is the signal source followed by the enabled resistor, Rx. The Rx (0 Ω 0402 SMD package) must be installed in order to enable the signal as clock to the probe. Please see "Clock routing technique" section for more details.

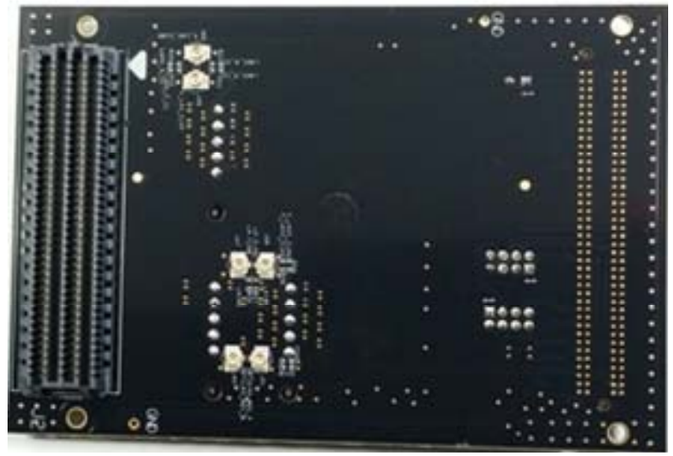
J7					
Assigned	Pin	Signal	Signal	Pin	Assigned
NC	1	NC	NC	2	NC
NC	3	NC	NC	4	NC
NC	5	CLK0	CLK1	6	NC
LA07-N	7	D15	D15	8	LA15-N
LA07-P	9	D14	D14	10	LA15-P
LA06-N	11	D13	D13	12	LA14-N
LA06-P	13	D12	D12	14	LA14-P
LA05-N	15	D11	D11	16	LA13-N
LA05-P	17	D10	D10	18	LA13-P
LA04-N	19	D9	D9	20	LA12-N
LA04-P	21	D8	D8	22	LA12-P
LA03-N	23	D7	D7	24	LA11-N
LA03-P	25	D6	D6	26	LA11-P
LA02-N	27	D5	D5	28	LA10-N
LA02-P	29	D4	D4	30	LA10-P
LA01-N - R21 *	31	D3	D3	32	LA09-N
LA01-P - R23 *	33	D2	D2	34	LA09-P
LA00-N - R20 *	35	D1	D1	36	LA08-N
LA00-P - R22 *	37	D0	D0	38	LA08-P
GND(Center Tab)					

* External IPEX J45, J46 feeds LA00-NP via R20/R22 or LA01-NP via R21/R23
R20, R21, R22, R23 are not populated.

J8					
Assigned	Pin	Signal	Signal	Pin	Assigned
NC	1	NC	NC	2	NC
NC	3	NC	NC	4	NC
NC	5	CLK0	CLK1	6	NC
LA23-N	7	D15	D15	8	LA31-N
LA23-P	9	D14	D14	10	LA31-P
LA22-N	11	D13	D13	12	LA30-N
LA22-P	13	D12	D12	14	LA30-P
LA21-N	15	D11	D11	16	LA29-N
LA21-P	17	D10	D10	18	LA29-P
LA20-N	19	D9	D9	20	LA28-N
LA20-P	21	D8	D8	22	LA28-P
LA19-N	23	D7	D7	24	LA27-N
LA19-P	25	D6	D6	26	LA27-P
LA18-N - R25 *	27	D5	D5	28	LA26-N
LA18-P - R27 *	29	D4	D4	30	LA26-P
LA17-N - R24 *	31	D3	D3	32	LA25-N
LA17-P - R26 *	33	D2	D2	34	LA25-P
LA16-N	35	D1	D1	36	LA24-N
LA16-P	37	D0	D0	38	LA24-P
GND(Center Tab)					

* External IPEX J47, J48 feeds LA17-NP via R24/R26 or LA18-NP via R25/R27
R24, R25, R26, R27 are not populated.

ZX182M-LPC Bottom



ZX182M-LPC Top

Note

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SPECIFIED DIMENSIONS ARE INCHES (MM).
ROHS COMPLIANT

ASSEMBLY DRAWING

ITEM: ZX182M-LPC

DESCRIPTION: FMC VITA 57.1 LPC test board Agilent Tektronix Mictor or Flying Leads probe passive mezzanine

CHECKED: M. MARINA

DRAWN: SLAVIK

REVISSION: 1.0

SHEET: 3 OF 3