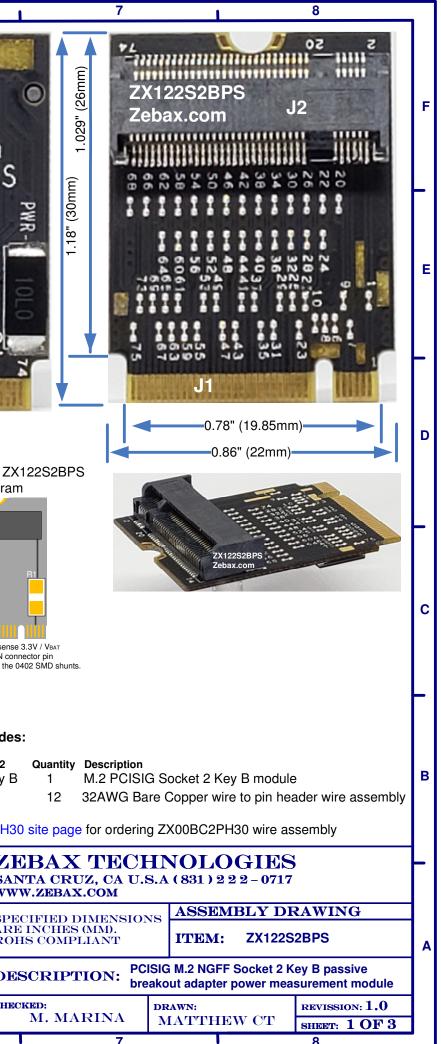
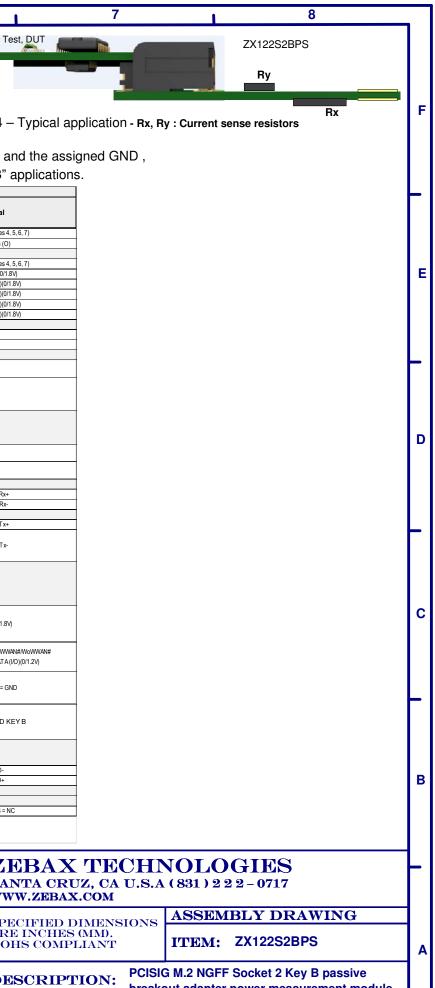
	1	1	2		3		4	5		6
	Product Name:	ZX122S2B	BPS PCISIG M.2		ey B passive I	breakout adap	ter, power mea	asurement module	and a start	
F	Product Descri			2 breakout adapter pr nent. ZX122S2BPS is			s as well as providi	ing method of power	0	
_	a) Ea b) Ea	ch PCISIG(ex ch 0402 SMD s	cluding GND signals shunt package may be	haracterization , test an ) are routed to 0402 S e wired for signal mea e cut and redirected to	MD shunt packag surement via scop	le for easy probe a be / test equipmen	access. It.	D shunt landing pads. bug.		X.com 2S2BPS
Е	a) Ea b) Util c) Util d) Ide	ch power suppl izing scope pro izing eLoad ( E ntify power sup	ly rail is designed with obe – test equipment Electronic Load ) , qua oply trace impedance,	ransients, Device Und current sensing powe , measure power supp lify host's power supp Rdc , for improved He	er resistor, please bly noise, ripples, ly & maximum ou	see block diagrar transients, and DL tput power.	n.	tion.	R1	Pg [
_	1- Provid 2- Onbo 3- Listed 4- All tra 5- Four	ard current ser I number adjac ces are 50 Oh ayers PCB des	ALL PCISIG signals v nse resistors for all su cent to each 0402 SM ms impedance contro sign, inner layers are	GND planes.	e table 1 for detail esents the associa	ated PCISIG M.2 o	connector's pin nun	nber.	2 N	R2
D	7- Mates	s with any key i	matching M.2 Host ar	g for ease of access f Id Device / DUT ng wires , ZX00BC2PI						
_	-	Frace impedan Operating Tem M.2 Edge Conr	perature: -65°C to + nector type(J1): Key : M.2 Key B		Figure 3- M.2 red	assembly , Z	Opper to pin header wire KOOBC2PH30 Zebax.com	Figure 2 – Ci	rcuit diagram	Figure 1 – Z Block diagram
С	r	M.2 Receptacle Key Type: H Height: 0.1 Spacer: 0. <sup>-</sup> Plating: Gc	e ( J2 ) : Key B 6" (4.2mm ) 1" (2.54mm) – See Fig old 100U	-		BPS Zebax.com	<u>د</u> <u>Rsense</u> " (0.5mm)		R2 10mΩ M ID package 0 Ω J1 designed 50 Ω trace impedance contr ptacle connector for the ZX122S2BPS	
-	(	Current Sense:	mΩ 2512 SMD 7W - T	) <sup>-</sup> hickness: 0.02" ( 0.5n	nm) Max - See Fi	gure 3	Compliance:			
в	S	Temperatur	re Coefficient: ±75ppr Femperature:-65°C to -65°C to	n / °C +85°C at 100% listed +170°C see section F				96	Part number ZX122S2BPS	package include PCB Edge J2 Key B Key E
			Table 1 lists onbo ISIG M.2 connector a	pard ZX122S2BPS cu ssignment	rrent sense resist	ors and	•	er IEC-61249-2.21 : 2003 2011/65/EU		ZX00BC2PH3
	Table 1 Current Sens	e Resistor	CISIG M.2 Connector pin number 2, 4,	PCISIG M.2 Supply Rail	Description	Package           (inch)         (mm)           2512         6432	Certificate of Co	mpliance for Radioactive mpliance for Asbestos mpliance for Ozone Deple		S SA WW
Α	R2 Notice		70, 72, 74	3.3 V/VBAT	10m Ohms 1% 7W	2512 6432		CH SVHC mpliance RoHS_EN_CoC ies no warranties, expressed,	) )	RO
	IMPLIED, STATUTORY, OR OTHE Information furnished is believed to	RWISE WITH RESPEC	T TO THE MATERIALS, AND EXPI e. However, Zebax Technologies as	RESSLY DISCLAIMS ALL IMPLIED	WARRANTIES OF NO INFRI equences of use of such info	NGEMENT, MERCHANTABIL rmation or for any infringemer	LITY, AND FITNESS FOR A PA	RTICULAR PURPOSE.		СНЕ
	1		2	Î	3	1	4	5	I	6



	1	2	3	4	5		1			6	
										Device Under Tes	
	Product Name: 7X12	292889 POISIG M 2 NGEE	Socket 2 Key B passive bre	akout adanter - now	ver measurement modul	<u>م _ F</u>	one	2 of 3	2		
			booker 2 key B passive bre				uge	2010	•		
F		ed. eLoad test equipment may be a	ors may be removed if external elect pplied to ZX122S2BPS for power su	ipply			0.14			Figure 4 –	
	characterization, te	est and measurements. Eload supp	liers : BK Precision , Chroma, Instek	, Kikusui and more	Table 2 – PCISIG M.2 So Table 2 represents only the P				2 Kev	B nower supply ar	
	Signal assignments:	Table 2 exhibits the routed M.2 PC	SIG signals on the ZX122S2BPS m	odule.	PCISIG M.2 reference ground, signal assignments for "Socket 2 Key B Socket2 PCIe / USB 3.1 Gen1-Based WWAN Key B						
	1- Table 2 represe	nts only the PCISIG M.2 Socket 2 I	Signal			2 connector 22S2BPS	Ϋ́.	Signal			
			ts for "Socket 2 Key B" applications.		3.3 VVBAT	<b>Pin</b> 74	Label <sup>1</sup>	Labe	1 Pin 75	CONFIG_2 (States 4, 5	
					3.3 VVBAT 3.3 VVBAT	72	R2 <sup>2</sup>	73		VIO_CFG (0)	
			Key B signal assignments for the liste		SUSCLK (I)(0/1.8 V/3.3 V)	68	68		69	GND CONFIG_1 (States 4, 5	
Ε	However; <b>ther</b>	SIM_DETECT (I) COEX_TXD (O)(0/1.8 V)	66 64	66 64	67 65	67 65	RESET# (I)(0/1.8) ANT CT L3 (O)(0/1.8				
			GND reference M.2 pin assignments		COEX_RXD (I)(0/1.8 V) COEX3 (I/O)(0/1.8 V)	62 60	62 60	61	63 61	ANT CT L2 (O)(0/1.8 ANT CT L1 (O)(0/1.8	
			oly your design signal name conven		NC	58	58	59	59	ANT CT L0 (0)(0/1.8	
	supply rail sign	hals as the listed signal names on t	ne Table 1 applies to the listed spec	ific M.2 application.	NC PEWAKE# (I/O)(0/1.8 V/3.3 V)	56 54	56 54	55	57 55	GND NC	
					CLKREQ# (I/O)(0/1.8 V/3.3 V)	52	52 50	53	53 51	NC GND	
		M.2 GND , reference ground , sign	hals are connected to each other alo		PERST# (I)(0/1.8 V/3.3 V) VENDOR DEFINED or GPIO_4 - TX_BLANKING/GNSS_1/UIM_PWR2/IPC_4 (I/O)(0/1.8V*)	50 48	48	49	49	NC	
	GND planes. In a rework and probi		ZX122S2BPS is the module's GND	for purpose of	VENDOR DEFINED or GPIO_3 - SYSCLK/GNSS_0/UIM_RST2/IPC_3 (I/O)(0/1.8V*)	46	46	47	47	NC	
D	PCISIG M.2 signal	VENDOR DEFINED or GPIO_2 - GNSS_IRQ/GNSS_IRQ/UM_CLK2/IPC_2 (VO)(0/1.8V*) VENDOR DEFINED or GPIO_1 -	44	44		45	GND				
			nals (excluding the power supply i		GNSS_SDA/GNSS_SDA/UM_DATA2/IPC_1 (VO)(0/1.8V*) VENDOR DEFINED or GPIO 0 -	42	42	43	43	NC	
	Onms Impedance	e controlled. ZX122S2BPS passes	through the reserved "NC" No Conn	ect signals as well.	GNSS_SCL/GNSS_SCL/SIM_DET2/IPC_0 (I/O)(0/1.8V*)	40	40	41	41	NC GND	
					UIM_PWR (0)	38	38 36	37	37	USB3.1-Rx+	
					UIM_DATA (I/O) UIM_CLK (O)	34	34 32	35	35 33	USB3.1-Rx- GND	
	Application: Bringup,	UIM_RESET (O)	30	30	31	31	USB3.1-Tx+				
	M.2 PCISIG Socke		VENDOR DEFINED or GPIO_8 - AUDIO_3/AUDIO_3/PLA_S2#/IPC_6-AUDIO_3 (I/O) (0/1.8V)	28	28	29	29	USB3.1-T x-			
	Socket 2 Add-in Ca	NWAN DP WIFI GPS GYRO Comp ard Key B-E , Socket 2 DisplayPo (ev C , Socket 2 PCIe-based SSD		SD Kev B-M	VENDOR DEFINED or GPI0_10 - W_DISABLE2#/W_ DISABLE2#/W_DISABLE2#/(VO)(0/1.8V)/HSIC_STROBE (VO) (0/1.2V)	26	26	27	27	GND	
С	Socket 2 PCIe / US Socket 2 USB3.1 0	VENDOR DEFINED or GPIO_7 - AUDIO_2/AUDIO_2/RFU/IPC_ 5-AUDIO_2 (I/O) (0/1.8V)	24	24	25	25	DPR (I)(0/1.8V)				
	Socket 3 PCIe-bas	VENDOR DEFINED or GPIO_6 - AUDIO_1/AUDIO_1/RFU/AUDIO_1 (I/O)(0/1.8V)	22	22	23	23	GPIO_11-WoWWAN#/WoWWAI (O)(0/1.8V)/HSIC_DATA(I/				
					VENDOR DEFINED or GPI0_5 - AUDIO_0/AUDIO_0/RFU/AUDIO_0 (//O)(0/1.8V)	20	20	21	21	CONFIG_0 = GNI	
	,	dard M.2 NGFF PCISIG connector	,		ADD-IN CARD KEY B	18 16 14	18 16 14	19 17 15		ADD-IN CARD KE	
		125 2199119 2199230 2199133 JA				14	14	15		-	
	Bellwethe	er: SD-80148 SD-80149 SD-80152	SD-80159 Amphenol		VENDOR DEFINED or GPIO_9 - LED_1#/LED_1#/LED_1# (O)(O)(0):3:3V) //PC_7 (I/O)(0/1.8V) W_DISABLE1# (I)(0/1.8 V/3.3V)	10 8	10 8	11	11	GND USB D-	
В		_			FULL_CARD_POWER_OFF# (I)(0/1.8V)	6	6	5	7	USB_D+ GND	
	Module Insertion, Re	-		t samman	3.3 V/VBAT	2	R1 <sup>2</sup>	3	3	GND	
	In order to avoid a	Note 1: Label is the labled number on the adjacent 0402 SMD s	shunt package	e on the ZX12	22S2BPS modu	e. The listed	CONFIG_3 = NC signal name in table 2 may vary				
	the below listed g	juidelines for insertion and removal	process:	Fig. 1	depending to your M.2 design configuration. Please appl 2: The supply power is available on the listed current senses		n signal name	e convention to	non-power su	uply rail signals & GND.	
	1 Nove the Med	ule against the housing chamber, s	oo figuro 1								
	2- Rotate module						SAN				
	3- Rotate the module						ww				
	4- Fix the module						SPE				
				Screw Fig. 4						ARE	
	Notice ALL ZEBAX TECHNOLOGIES DESIGN SPECIFI	ICATIONS, DRAWINGS, PUBLICATIONS. AND OTHER	DOCUMENTS (TOGETHER AND SEPARATELY, "MATERI	Fig. 5	ZEBAX MAKES NO WARRANTIES, EXPRESSED	,				DE	
	IMPLIED, STATUTORY, OR OTHERWISE WITH Information furnished is believed to be accurate a	RESPECT TO THE MATERIALS, AND EXPRESSLY DIS and reliable. However, Zebax Technologies assumes no re	CLAIMS ALL IMPLIED WARRANTIES OF NO INFRINGEM	ENT, MERCHANTABILITY, AND FITNES	S FOR A PARTICULAR PURPOSE. er rights of third parties that may result from its use					CHEC	
			Il other information previously supplied. Zebax Technologies								

-1



breakout adapter power measurement modul							
IECKED:	DRAWN:	REVISSION: 1.0					
M. MARINA	MATTHEW CT	SHEET: 2 OF 3					
7		8					

	1	1	2	3		4		5	6	
	Product Name: ZX12	22S2BPS PCIS	IG M.2 NGFF Sod	cket 2 Key B passi	ive breakout	adapter - pow	ver measuremer	nt module – Page 3 c	of 3	
F	Typical Application:	ZX122S2BPS is designed for purpose of PCISIG M.2 power supply characterization, test and debug at full connector's bandwidth. It provides onboard current sense resistors where scope probe could be utilized for measuring characterization data for qualifying the host or device functional behavior. Additionally, the current sense resistors may be replaced by eLoad for transient and dynamic load throttling. Below are few suggestions in respect to proper power supply measurements using ZX122S2BPS module:								
11	Scope Probe wire I	notallation						Keysight Probe He	ad accessories	
E	Utilize tł scope +	ne supplied ZX00BC probing options, in	stall probe wire as lis			– Based on avai	lability of type of	InfiniiMax RC Probe Heads	InfiniiMax II Probe Heads	
	2- In ord refere	ecommended to kee ler to avoid ground l nce. ZX122S2BPS p re scope probe's ba	MX0103A Bullet Ada MX0106A Diff. Solder-In							
-	indus 3- Both below	N2839A Diff. Browser	N5425B ZIF							
D	4- Pleas	probe, N5426A b) Tektronix offers P6247 or any T	ZIF Tip, N2884A Find several single-ended P1500, TAP2500, TA	N2795A, N2796A, 116 e Wire ZIF Tip and more d as well as differential AP3500, TAP4000, P72 ation of probe wires & a	e – See the figur probes such as : 240 of TDP7000 :	e "probe head ac P6243, P6245, F	cessories". 26248, P6246,	MX0105A Diff. SMA		
-	operatin highly re <b>above</b> 8	g within -65°C to 85 ecommended to utiliz 85°C test environme	°C temperature range ze external cooling fa nt.	PS module are designe e. The current sense re n if your design expects	sistor's power ra s to exceed maxi	ting will degrade mum current via	at above 85°C test e each PCISIG M.2 p	environment. It is	Tektronix P6243 sco	
с	The onb R1, R2 The onb									
	The onboard current sense resistors <b>power ratings</b> derail at <b>above</b> 85°C. Figure 4 exhibits the current sense resistors derating curve. Current sense resistors rated power ; P = VI = I**2 x R where I is the maximum current for the listed resistor value R Below are few suggestions, if your test & measurement environment falls ≥ <b>+85°C</b> temperature range :									
В	prov 2- Repla 3- Repla	vides heatsink soluti ace the onboard curr ace onboard current	on to the onboard cu ent sense resistors w	stor's terminal blocks a rrent sense resistors via vith lower values ( simila eLoad ( electronic Load dation.	a inner layers the ar footprint ), res	ermal distribution ulting at higher po	method. ower ratings at ≥ 85°	°C test environment.		
	Figure 4 – Current	sense resistor Deratir								
	80 60 1 1 1 20 40 1 20 40 40 40 40 40 40 40 40 40 4									
Α	-65	20 40 60 80; 100 120 85 esistor terminal – Temperature °C	140 160 180 170						SPH ARI ROI	
	ALL ZEBAX TECHNOLOGIES DESIGN SPECI IMPLIED, STATUTORY, OR OTHERWISE WIT	TH RESPECT TO THE MATERIA	LS, AND EXPRESSLY DISCLAIMS	SALL IMPLIED WARRANTIES OF NO	INFRINGEMENT, MERCH	ANTABILITY, AND FITNESS	S FOR A PARTICULAR PURPOS	SE.	DE	
	Information furnished is believed to be accurate Specifications mentioned in this publication are							esult from its use.	CHE	
	1		2	3	ĺ	4		5	6	

