	1	1	2	1	3		4	1	5		6	
	Product Name:	ZX120	GT – PCISIG min	i PCle passiv	ve breakout ext	tender adap	ter					
F	Product Descri	ZX120G test and All reser	ZX120GT is a mini PCIe passive breakout extender adapter module, providing access to all mini PCIe signals. ZX120GT mates with host. It is designed for real-time Test & Measurement, signal integrity, characterization, manufacturing test and debug of any mini PCIe design interface. All reserved mini PCIe Ground signals are inner connected to GND planes as well as GND stitching vias. It is available at the GND Test Points, TP, and the Mounting Holes, MH.							Figure 1 Circuit diagram		
E	 1- Provides access to ALL mini PCIe PCISIG signals via standard through hole, TH, test points. 2- ZX120GT is designed to be inserted into the host for purpose of debugging, development, testing and characterization. 3- Listed number adjacent to each TH test point represents the associated mini PCIe connector's pin number. 4- All traces are 50 Ohms impedance controlled with exceptional signal integrity & crosstalk. 5- Four layers PCB design, inner layers are GND planes with direct connection to GND stitching vias & top/bottom GND fills + the mounting holes. 6- Mates with any standard mini PCIe connector. 								nting holes.	50 Ω : All traces are designed 50 Ω trace impedance control J1 : mini PCIe PCISIG edge connector GND – All reserved mini PCIe Ground signals are inner connec planes as well as GND stitching vias. It is available at the GND TP, and the Mounting Holes MH		
-	Electrical: Insertion loss > -2dB @3GH2 TP, and the Mounting Holes, MH. Trace impedance: 50 Ω Operating Temperature: -65°C to +170°C Figure 2 – ZX120GT Circuit d mini PCIe Edge Connector type (J1): mini PCIe, 52 position Plating: Gold 75U Through Hole Test Point : The description of the section of the sect									cuit diagram		
D		Plating: Gold	andard 0.1" (2.54mm 75U n: 0.5A (maximum)) post - 0.025" (0.064mm) diamete	er				ZX120GT	тр. мн О О	GND
_	Application: Bringup, testing, emulation, development, modular design evaluations, manufacturing loopback test, 50 Ω : All traces are designed 50 Ω tr J2 : mini PCIe PCISIG receptacle con Wifi GPS GYRO Compass BT FM sensor GND – All reserved mini PCIe Ground TP, and the Mounting Holes, MH.										CISIG receptacle connected mini PCIe Ground sign GND stitching vias. It is	ctor nals are inner connecte
	Mates with: Any with any standard mini PCIe PCISIG host and device – TE 1775861 Molex SD-48338 and more Table 1 – Standard PCI									Signal assignr	nents	
с		round : All reserved mini PCIe Ground signals are inner con Access to the GND is available at the GND Test Poin Please refer to table 1 for list of the reserved GND sidesignated TH test point.				· · · · · · · · · · · · · · · · · · ·			k Name Reserved Reserved Reserved Reserved GND +3.3Vaux	Pin # 52 50 48 46 44 42	Name +3.3Vaux GND +1.5V LED_WPAN# LED_WLAN# LED WWAN#	- - - - -
_								39 37 35 33 33	+3.3Vaux GND GND PETp0 PETn0	40 38 36 34 32	GND USB_D+ USB_D- GND SMB_DATA	- - - - - Orderir
в					European Uni	fied Free locument Directive (Directive on Directive (203/	11/EC)	29 27 25 23 21 19	GND GND PERp0 PERn0 GND Reserved* (UIM_C4)	30 28 26 24 22 20	SMB_CLK +1.5V GND +3.3Vaux PERST# W_DISABLE#	Orderir Part nun ZX120G
					RoHs Directive	per IEC-61249-2.2 e 2011/65/EU ve (2012/12/EU)	21 : 2003	17		18 echanical Key	GND	
					Certificate of 0 Certificate of 0 Certificate of 0 Certificate RE	Compliance for Rac Compliance for Ast Compliance for Ozo ACH SVHC	one Depleting Substances, C	5	GND REFCLK+ REFCLK- GND CLKREQ# COEX2	16 14 12 10 8 6	UIM_VPP UIM_RESET UIM_CLK UIM_DATA UIM_PWR 1.5V	- ZH - SAN - WW - SPE - ARE
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	1		2		3		4	1	5		6	

