

DOCUMENT : <u>ZX200-AC2-N1080A</u>

SUBJECT: ZX200 Vs Agilent N1080A

Comparison test case study using Zebax ZX200 vs. Agilent N1080A HDMI test fixture (aka. Test board)

The subsequent pages are full test record using Zebax ZX200 HDMI test fixture

Test Case : **4Kx2K 30 Hz PRN** HDMI Clock Frequency: **2.96GHz**

Full comparison chart can be found here:

ZX200-vs-Agilent-4Kx2K-ZXTR-ZX200-AC2-N1080A.pdf





HDMI Test Report

Overall Results:0 of 20 Tests Failed

Test Configuration Details				
Dev	vice Description			
Device Name Quantum 804A				
Comments	Zebax fixture 3 4kx2k 30Hz PRN run 1			
Device ID	Transmitter			
ConnectionType	4 Connections 1.4			
HDMI Specification				
Test Fixture Type	Other			
Test	Session Details			
Infiniium SW Version	05.71.0000			
Infiniium Model Number	DSO81204B			
Infiniium Serial Number	MY46002010			
Application SW Version	1.03.9002			
Last Test Date	3/29/2013 10:39:58 AM			

Summary of Results

Margin Thre	esholds
Warning	< 2 %
Critical	< 0 %

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Spec Range
1	0	1	7-9: Clock Jitter	164mTbit	34.4 %	VALUE <= 250mTbit
1	0	1	<u> 7-10: D0 - Mask Test</u>	0.000	50.0 %	No Mask Failures
1	0	1	<u> 7-10: D0 - Data Jitter</u>	205m	31.7 %	<=0.3Tbit
1	0	1	<u> 7-10: D1 - Mask Test</u>	0.000	50.0 %	No Mask Failures
1	0	1	<u> 7-10: D1 - Data Jitter</u>	207m	31.0 %	<=0.3Tbit
1	0	1	<u> 7-10: D2 - Mask Test</u>	0.000	50.0 %	No Mask Failures
1	0	1	<u> 7-10: D2 - Data Jitter</u>	193m	35.7 %	<=0.3Tbit
1	0	1	7-4: Clock Rise Time	167.830ps	123.8 %	VALUE >= 75.000ps
1	0	1	7-4: Clock Fall Time	178.160ps	137.5 %	VALUE >= 75.000ps
1	0	1	<u> 7-4: D0 - Rise Time</u>	93.570ps	24.8 %	VALUE >= 75.000ps
1	0	1	<u> 7-4: D0 - Fall Time</u>	91.620ps	22.2 %	VALUE >= 75.000ps
1	0	1	<u> 7-4: D1 - Rise Time</u>	94.190ps	25.6 %	VALUE >= 75.000ps
1	0	1	<u> 7-4: D1 - Fall Time</u>	89.400ps	19.2 %	VALUE >= 75.000ps
1	0	1	<u> 7-4: D2 - Rise Time</u>	92.230ps	23.0 %	VALUE >= 75.000ps
1	0	1	<u> 7-4: D2 - Fall Time</u>	94.290ps	25.7 %	VALUE >= 75.000ps
1	0	1	7-8: Clock Duty Cycle(Minimum)	49.440	23.6 %	>=40%
1	0	1	7-8: Clock Duty Cycle(Maximum)	50.370	16.1 %	<=60%
1	0	1	7-6: Inter-Pair Skew - D0/D1	600µTpixel	49.8 %	-200mTpixel <= VALUE <= 200mTpixel
-	0	1	7-6: Inter-Pair Skew - D0/D2	500µTpixel	49.8 %	-200mTpixel <= VALUE <= 200mTpixel
-	0	1	7-6: Inter-Pair Skew - D1/D2	100µTpixel	50.0 %	-200mTpixel <= VALUE <= 200mTpixel

Report Detail

7-9: Clock Jitter				
				Reference: Test ID 7-9
Recovery Clock. For compliance, the D	Dition: 4 Channels Connection Mo DUT should output 27MHz(or 25MH lock Jitter 164mTbit			*Tbit, relative to the ideal
Result Details				
Test Frequency(MHz) 297.081	# Edges 16.00000000M	Tbit(ps) 336.609	Clock Jitter(ps) 55.070	·
Trial 1				
Trial 1: Clock Jitter				
Ax				
			and the second	
		and the second	No. of Concession, Name of Conce	
Ay			e en	:BY
Scales Channe	Horiz Scale Position 1 1 16.80ps/div 0.000s	170.0mV/div 6.0	 Eset 000mV	BX
7-10: D0 - Mask 7	on 4 16.80ps/div 0.000s	170,0mV/div 6.(]00mV	
Y 7-10. D0 - Wask	1651			Reference: Test ID 7-10
Test Descrip	tion: For all channels under all c	operating conditions spec	cified in Table 4-11 . The Source	
Test Summary: Pass				
Test Limits: No Mask Failures	-			
Result Details	J []			
Maximum Margin 0.000000000	000s Maximum Margin (Ve	rtical) 0.000000000	000V Test Frequency(N	/Hz) 297.081
Mask Moved(ps) 0.000 # Acq	uisitions Point 16.0000000	00M Tbit(ps) 336.	725 RightJitterData(Tb	i t) 205m
LeftJitterData(Tbit) 202m Rig	htJitterData(ps) 68.900	eftJitterData(ps) 68	Differential Swing	y Voltage(V) 945m
Mask Revision RevB				
Trial 1				

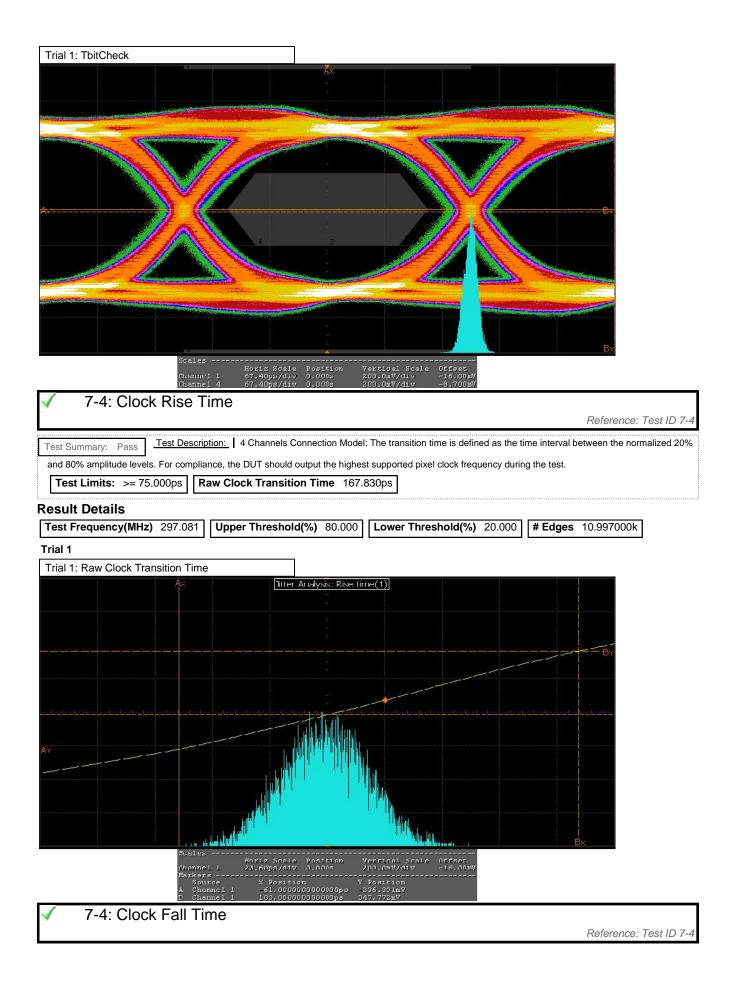
Trial 1: Total # failures		
	le Position Vertical Scale Offset	
Channel 2 67.40ps/div	iv 0.000⊱ 200.0mV/div -16.00mV iv 0.000s 200.0mV/div 44.10mV	
7-10: D0 - Data Jitter	Reference: Test ID	7-10
Test Summary: Pass Test Description: For all channel TP1, which meet the normalized eye diagram requirements. Test Limits: <=0.3Tbit TbitCheck 205m		∍ls at
Result Details		
Test Frequency(MHz) 297.081 Mask Moved(ps)	* Acquisitions Point 16.00000000M * Tbit(ps) 336.725	
For all channels under all operating conditions specified in Table 4-11. The Source shall have output levels at TP1, which meet the normalized eye diagram requirements. Test Summary: Pass Test Summary: For all channels under all operating conditions specified in Table 4-11. The Source shall have output levels at TP1, which meet the normalized eye diagram requirements. Test Summary: Test Description: Test Description: Test Description: Summary: Test Description: Summary: Test Description: Summary: Test Description: Test Description: Summary: Test Description:		
Differential Swing Voltage(V) 945m Mask Revis	vision RevB	

Trial 1: TbitCheck			
	Āx - -	and the second secon	
			Bx
Scales Horic Scale Channel 1 67,40ps/diy Channel 2 67,40ps/diy	v 0.000s 200.0mV/div	 le Offset -16.00mV 44.10mV	
7-10: D1 - Mask Test			Reference: Test ID 7-10
Test Summary: Pass Test Description: For all channel TP1, which meet the normalized eye diagram requirements. Test Limits: No Mask Failures Total # failures	·	ns specified in Table 4-11 . The	Source shall have output levels at
Result Details			
Maximum Margin 0.000000000000 Maximum	Margin (Vertical) 0.0000	D0000000V Test Freque	n cy(MHz) 297.081
Mask Moved(ps) 0.000 # Acquisitions Point 1	6.000000000M Tbit(ps)	336.688 RightJitterDa	ta(Tbit) 207m
LeftJitterData(Tbit) 205m RightJitterData(ps)	69.650 LeftJitterData(p	bs) 68.900 Differential	Swing Voltage(V) 917m
Mask Revision RevB			
Trial 1			

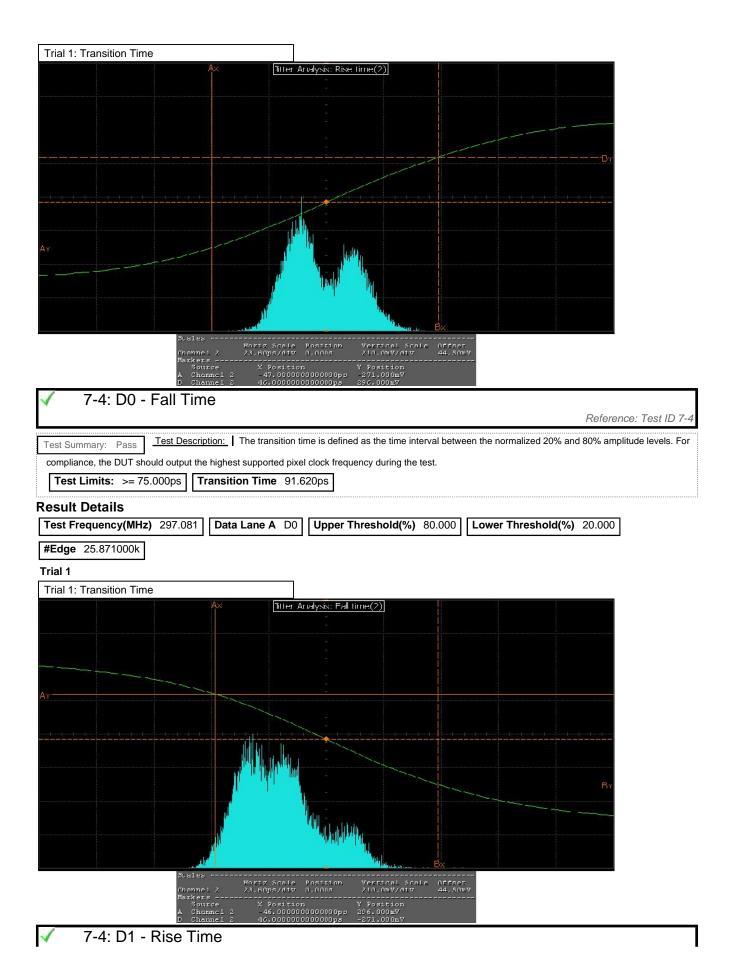
Trial 1: Total # failures						
	ξx -					
					and the second second	
	2					
Scales Horic Scale Channel 1 67.40ps/diy Channel 3 67.40ps/diy	v 0.000s	Vertical Scale 200.0mV/div 200.0mV/div	Offset -16.00mV 12.80mV		: 0.8	
7-10: D1 - Data Jitter						
						ce: Test ID 7-10
Test Summary: Pass Test Description: For all channel	els under all o	perating conditions	specified in T	able 4-11. The	e Source shall hav	/e output levels at
TP1, which meet the normalized eye diagram requirements.						
Test Limits: <=0.3Tbit TbitCheck 207m						
Result Details						
Test Frequency(MHz) 297.081 Mask Moved(ps	s) 0.000 #	# Acquisitions P	Point 16.00	M000000M	Tbit(ps) 336.	.688
RightJitterData(Tbit) 207m LeftJitterData(Tbit)	205m R	ightJitterData(p	s) 69.650	LeftJitterD	Data(ps) 68.90	0
Differential Swing Voltage(V) 917m Mask Revis	sion RevB]				—

Trial 1: TbitCheck				_
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	-			
	-		В	×
Scales Horiz Scale Channel 1 67.40ps/div Channel 3 67.40ps/div	v 0.000s 200.0	cal Scale Offset uV/div -16,00mV uV/div 12,80mV		_
7-10: D2 - Mask Test				
			Refere	ence: Test ID 7-10
Test Summary: Pass Test Description: For all channel		conditions specified in	Table 4-11 . The Source shall h	nave output levels at
TP1, which meet the normalized eye diagram requirements.				
Test Limits: No Mask Failures	s 0.000			
Result Details				07.004
	Margin (Vertical)		Test Frequency(MHz) 2	
Mask Moved(ps) 0.000 # Acquisitions Point 1	6.00000000M	bit(ps) 336.694	RightJitterData(Tbit) 193	ßm
LeftJitterData(Tbit) 193m RightJitterData(ps)	65.150 LeftJitter	Data(ps) 65.150	Differential Swing Voltag	ge(V) 901m
Mask Revision RevB				
Trial 1				

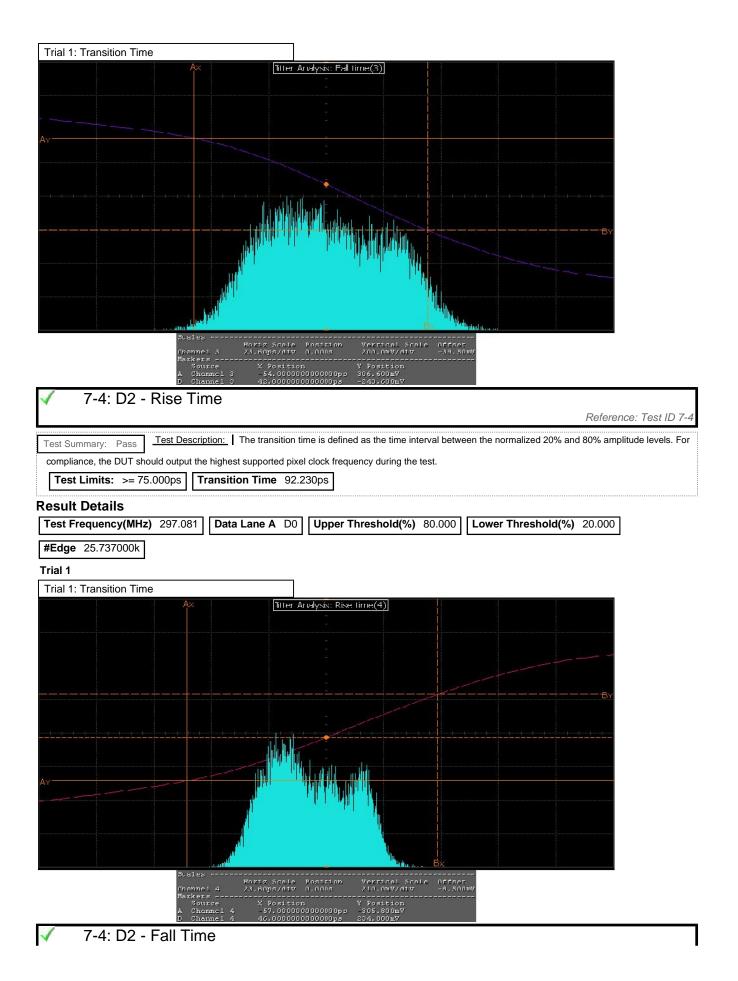
Trial 1: Total # failures	
Scales	v 0.000≿ 200.0mV/div −16.00mV
7-10: D2 - Data Jitter	
	Reference: Test ID 7-10
Test Summary: Pass <u>Test Description:</u> For all channe	els under all operating conditions specified in Table 4-11 . The Source shall have output levels at
TP1, which meet the normalized eye diagram requirements.	
Test Limits: <=0.3Tbit TbitCheck 193m	
Result Details	
Test Frequency(MHz) 297.081 Mask Moved(ps)	b) 0.000 # Acquisitions Point 16.00000000M Tbit(ps) 336.694
RightJitterData(Tbit) 193m LeftJitterData(Tbit)	193m RightJitterData(ps) 65.150 LeftJitterData(ps) 65.150
Differential Swing Voltage(V) 901m Mask Revis	ision RevB



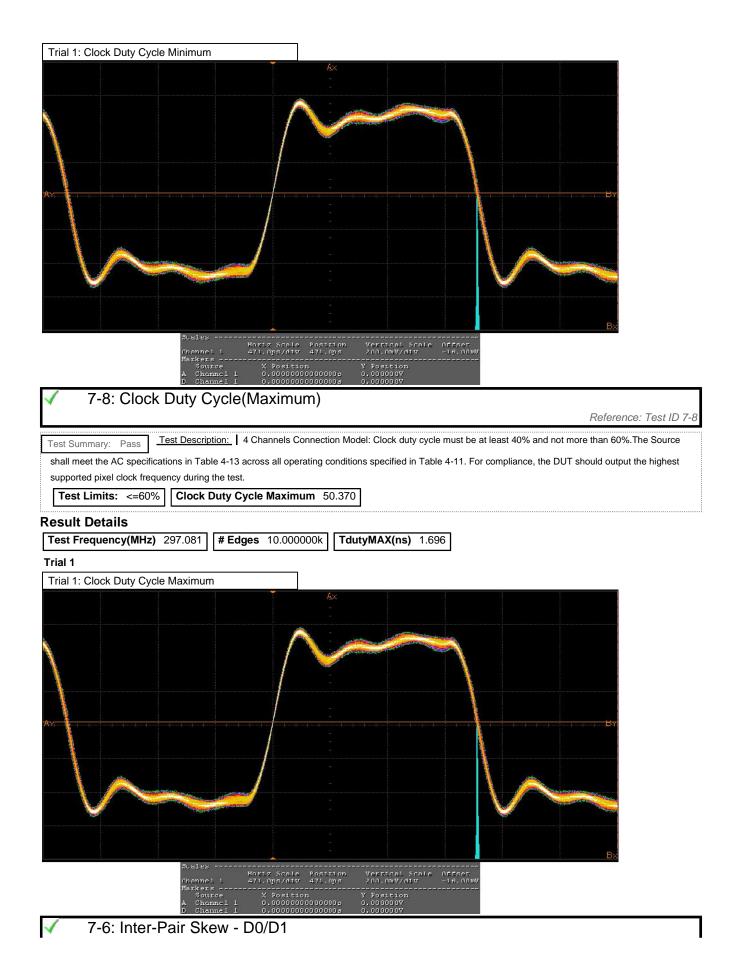
Test Summary: Pass Test Descrip	otion: 4 Channels Conn	ection Model: Th	e transition time is	defined as the time	interval between the nor	malized 20%
and 80% amplitude levels. For complia	nce, the DUT should outp	out the highest su	oported pixel clock	frequency during the	he test.	
Test Limits: >= 75.000ps	aw Clock Transition	Time 178.160	os			
Result Details						
Test Frequency(MHz) 297.081	Upper Threshold(%	b) 80.000 L	ower Threshold	I(%) 20.000 #	Edges 10.996000k]
Trial 1						-
Trial 1: Raw Clock Transition Time	:					
	litter Anz	alysis: Fall time(1) -				
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Channe Narker	1.1 23.60ps/div 0	osition Vert .000s 200.	ical Scale Offs DmV/div -16.			
Sou A Cha	rce X Position mmcl 1 0.000000000		000V			
✓ 7-4: D0 - Rise Tin	nnel 1 0.000000000	000005 0.000	900V			
	lie				Pafaranca	Test ID 7-4
Test Summary. Fass	otion: The transition time			ween the normalize	d 20% and 80% amplitud	le levels. For
compliance, the DUT should output the			uring the test.			
Test Limits: >= 75.000ps	ransition Time 93.57	Ups				
Result Details						
Test Frequency(MHz) 297.081	Data Lane A D0	Upper Thresh	old(%) 80.000	Lower Thres	hold(%) 20.000	
#Edge 25.514000k						



			Referen	ce: Test ID 7-
Test Summary: Pass Test Descrip	tion: The transition tir	ne is defined as the time interval betw	een the normalized 20% and 80% amplit	ude levels. For
compliance, the DUT should output the				
Test Limits: >= 75.000ps	ansition Time 94.1	90ps		
esult Details				
Test Frequency(MHz) 297.081	Data Lane A D0	Upper Threshold(%) 80.000	Lower Threshold(%) 20.000	
#Edge 24.764000k				
rial 1				
Trial 1: Transition Time				
	Ax Titter Ar	alysis: Rise time(3)		
			B _Y	
		J.		
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Y				
	a 23.60ps/d1w ce X Position mcl 3 - 44,000000 mel 3 50.0000000	000000ps -243.600mV		
	5		Referen	ce: Test ID 7
Test Summary: Pass Test Descrip	tion: The transition tir	ne is defined as the time interval betw	veen the normalized 20% and 80% amplit	ude levels. For
compliance, the DUT should output the	highest supported pixel	clock frequency during the test.		
	ansition Time 89.4			
esult Details				
Test Frequency(MHz) 297.081	Data Lane A D0	Upper Threshold(%) 80.000	Lower Threshold(%) 20.000	
#Edge 25.726000k	L]			
rial 1				

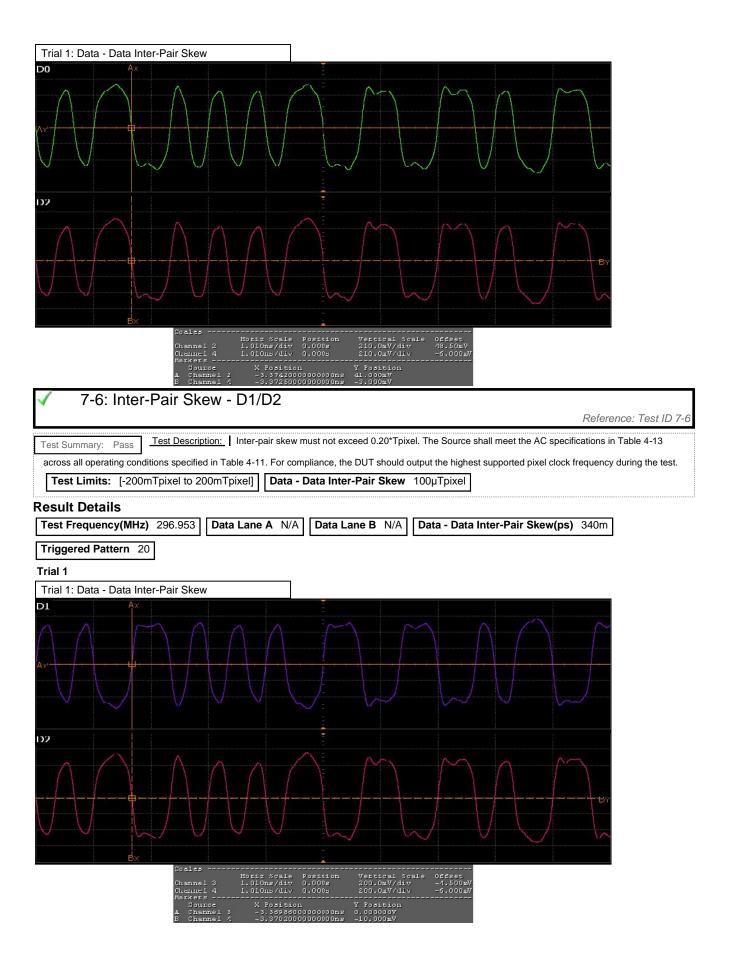


Test Decrir	tion: The transition tim	he is defined as the time in	torval botw	Reference	
est Summary: Pass				een me normalizeu 20 % and 60 % amplituu	e levels. I U
· · ·	ansition Time 94.29		1651.		
esult Details					
est Frequency(MHz) 297.081	Data Lane A D0	Upper Threshold(%)	80.000	Lower Threshold(%) 20.000	
Edge 24.862000k					
ial 1					
rial 1: Transition Time					
	Ax Titter An	alysis: Fall time(4)			
landana kana kana kana kana kana kana kan			l	perspendamentan perspectation perspectation and the second s	
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		The manufacture of the second se	e B×		
B Cha	Horiz Scale F 1 4 23.6 hps/div f 8	210.0mV/d1v V Position 000000ps 234,800mV 00000ps -005.000mV	ule Offsei –8.50		
7-8: Clock Duty C	sycle(Minimum)		Reference	: Test ID
est ourinnary. T ass	le 4-13 across all operati	-	-	be at least 40% and not more than 60%.Th For compliance, the DUT should output the	e Source
Test Limits: >=40%	Duty Cycle Minimum	49.440			
esult Details					
est Frequency(MHz) 297.081	# Edges 10.00000	0k TdutyMIN(ns) 1	664		



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					Reference: Test ID
Test Summary: Pass	Test Description: Inter-pair s	skew must not exceed 0	20*Tpixel. The Source s	hall meet the AC specific	ations in Table 4-13
	ions specified in Table 4-11. Fo			t supported pixel clock fre	equency during the test.
Test Limits: [-200m	Tpixel to 200mTpixel]	ata - Data Inter-Pair	Skew 600µTpixel		
Result Details					
Test Frequency(MHz)	297.081 Data Lane A	N/A Data Lane B	N/A Data - Data	Inter-Pair Skew(ps)	1.960
Triggered Pattern 20	1				
Frial 1	1				
Trial 1: Data - Data Inte	r-Pair Skew	7			
	Channel 3 1.010ns/ Markers	/div 0.000s 210.	OmV		
7-6: Inter-	Pair Skew - D0/D2	2			Reference: Test ID
Test Summary: Pass	Test Description: Inter-pair s	skew must not exceed 0	20*Tpixel. The Source s	hall meet the AC specific	ations in Table 4-13
	ions specified in Table 4-11. Fo	or compliance, the DUT	should output the highes	t supported pixel clock fre	equency during the test.
Test Limits: [-200m	Tpixel to 200mTpixel]	ata - Data Inter-Pair	Skew 500µTpixel		
Result Details					
Test Frequency(MHz)	297.081 Data Lane A	N/A Data Lane B	N/A Data - Data	Inter-Pair Skew(ps)	1 700
Triggered Pattern 20	J				
Trial 1					



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