Product Name: **ZX181V-HSPC FMC+ HSPC Vita 57.4 breakout adapter – passive FPGA Mezzanine Card HSPC**

Product Description:

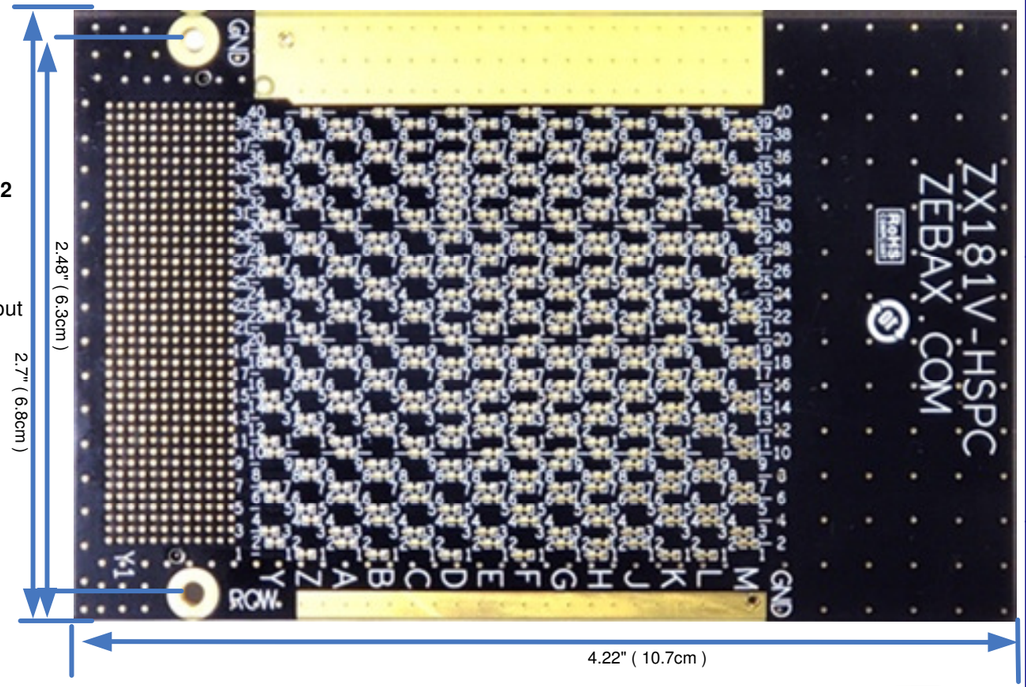
FPGA Mezzanine card , FMC+ , passive test module meeting VITA 57.4 standard bus interface. Includes 14 rows x 40 pins, totaling **560** pins, High Serial Pin Count, HSPC connectors supporting both Terminal (Mezzanine side) interfacing with host.

Full access to all (excluding the GND signals) Vita 57.4 HSPC signals via onboard 0402 SMD footprint. Please see **Page 2** for full list of accessible signals as listed by Vita 57.4 standard. The Vita57.4 assigned GND signals are not accessible individually, they are connected to inner GND planes as well as top/bottom layers fill. The GND access point is offered by 2 onboard GND test points and the exposed copper on the TOP layer interfacing with test equipment, debug & development.

Provides prototype area as well as onboard SMD 0402 footprint for accessing any of the Vita 57.4 signals. Ideal breakout mezzanine card for any design utilizing HSPC (14x40) connector series as well as Vita 57.4 standard design.

Fully compatible with **Vita 57.4 (FMC+ HSPC).**
Mates with Samtec Molex HI-SPEED HI-DENSITY SEARRAY HSPC design connectors.

- **Fully** compatible with 14 rows x 40 pins per row single ended or differential pairs design configuration
- Designed in 14 layers PCB stackup
- **All** signals are accessible via onboard standard 0402 SMD footprint.
- All signals (via 0402 SMD package) are pass through, enabling user to implement design changes (cut signal path), if design changes are required.
- Ideal mezzanine card for loopback applications.
- Improved signal integrity and crosstalk
- Multiple GND test points connecting directly to inner layers GND planes.
- Includes both HSPC , Terminal and Socket connectors
- Matching connector's **50Ω** trace impedance on all signals – Reference plane impedance 50Ω for DC to 10GHz bandwidth applications



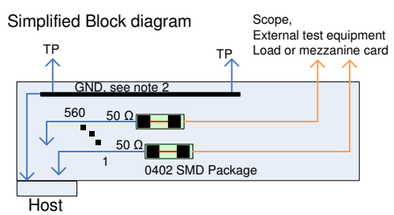
Application: FMC+ VITA 57.4 , Vita 57.4 FMC+ HSPC , daughter card Bringup, testing, emulation, Xilinx development interface testing daughter board to host, modular design evaluations

Access: All signals (excluding the GND signals of Vita 57.4 standard) are accessible via onboard 0402 SMD footprint.

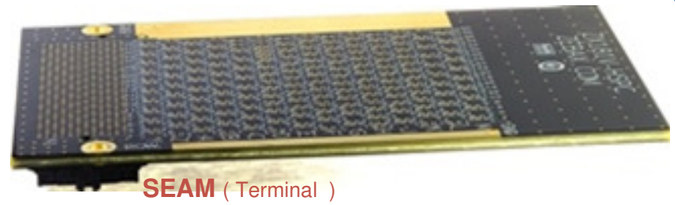
Pitch: 1.27mm (0.05") High Speed connector

Mates with : Xilinx FPGA development systems connecting daughter board to Host
Any and all FMC+ High Serial Pin Count, HSPC , VITA 57.4 compliant design.
ASP-184329-01 ASP-208573-01 Table below lists connectors compatible with ZX180-HSPC
FMC+ HSPC Vita 57.4 breakout adapter – passive FPGA Mezzanine Card HSPC

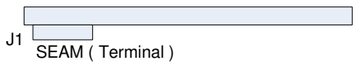
Simplified Block diagram



Note:
1- Prototype, Evaluation board, daughter card, Mezzanine card can be wired to ZX181V-HSPC
2-All Vita 57.4 signals are accessible.
3- All Vita 57.4 reserved GND signals are accessible via GND Test points.



ZX181V-HSPC , Passive FMC
VITAL 57.4 breakout adapter



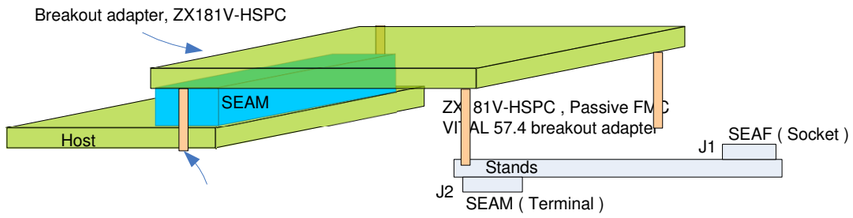
Note:
1- SEAM (Terminal) connector type interfaces with HOST.

Typical signal connection:
0402 SMD Package

Break signal path:

See Page 2 for more details

Note
ALL ZEBAX products are **RoHS** compliant and **Lead Free** unless otherwise indicated.



Note:
1- SEAM (Terminal) connector type interfaces with HOST
2- SEAF (Socket) connector type interfaces with Mezzanine Card.

ZX181V-HSPC FMC+ HSPC breakout adapter mates with the following Samtec SEARAY™ VITA 57.4 Connectors

Samtec PN	VITA 57.4	Description	Mated Stack Height
ASP-184329-01	HSPC	Socket	Standard height
ASP-208573-01	HSPC	Socket	Standard height

Socket : Also known as Female, is usually located on Host or Carrier Side.

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SPECIFIED DIMENSIONS ARE INCHES (MM).
ROHS COMPLIANT

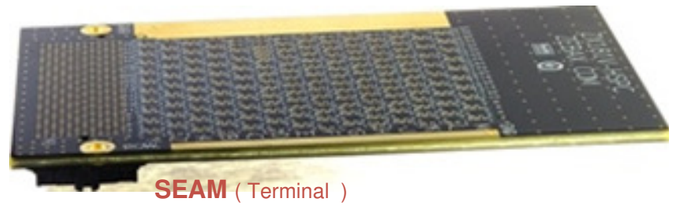
ASSEMBLY DRAWING

ITEM: ZX181V-HSPC

DESCRIPTION: **FMC+ HSPC VITA 57.4 breakout adapter – passive FPGA mezzanine card**

CHECKED: M. MARINA
DRAWN: SLAVIK
REVISSION: 1.0
SHEET: 1 OF 3

Product Name: **Cont's ZX181V-HSPC FMC+ HSPC Vita 57.4 breakout adapter – passive FPGA Mezzanine Card**
HSPC



Ground:

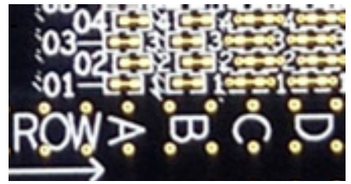
ZX181V-HSPC is breakout adapter – test module , offering VITA 57.4 signals. It enables user to implement design changes (cut signal path) , or simply access the Vita 57.4 signals for test and measurement purpose.

The GND access points are offered by 2 onboard GND test points interfacing with test equipment, host and target. It is connected to the module inner GND planes and top & bottom GND fills.

Access signals:

ZX181V-HSPC provides access to all Vita 57.4 signals. Table below lists the Vita 57.4 signals.

0402 landing pads



Vita 57.4 (FMC+ - HSPC) 14 x 40

Vita 57.1 (FMC - HPC) 10x40

Vita 57.1 (FMC - LPC) 4x40

Pin	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HBPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17-P-CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17-N-CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00-P-CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00-N-CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06-P-CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06-N-CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10-P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10-N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14-P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14-N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND
FMC LPC					X	X			X	X				
FMC HPC			X	X	X	X	X	X	X	X	X	X		
FMC+ HSPC	X	X	X	X	X	X	X	X	X	X	X	X	X	X

FMC LCP : Vita 57.1 Low Pin Count , LPC, signals
FMC HPC : Vita 57.4 High Pin Count, HPC , signals.
FMC+ HSPC : FMC+ High Serial Pin Count, HSPC , signals.

Note

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SPECIFIED DIMENSIONS ARE INCHES (MM).
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ASSEMBLY DRAWING

ITEM: ZX181V-HSPC

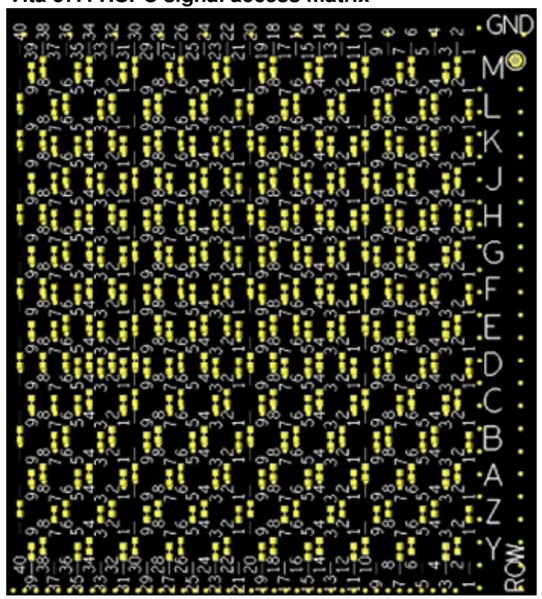
DESCRIPTION: **FMC+ HSPC VITA 57.4 breakout adapter – passive FPGA mezzanine card**

CHECKED: M. MARINA
DRAWN: SLAVIK
REVISSION: 1.0

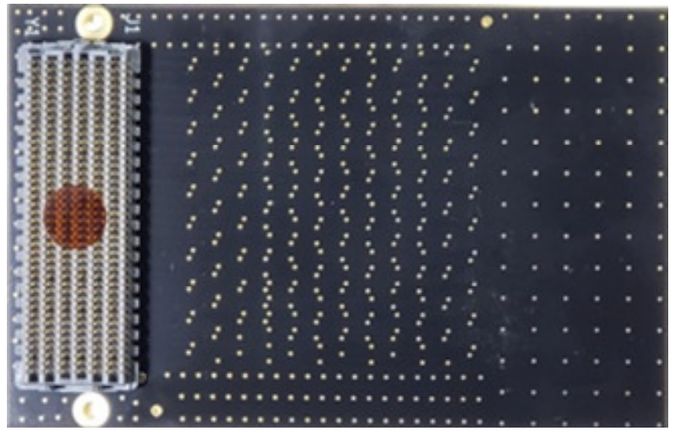
Product Name: **Cont's ZX181V-HSPC FMC+ HSPC Vita 57.4 breakout adapter – passive FPGA Mezzanine Card**
HSPC

Access point: All the Vita 57.4 signals are accessing via onboard 0402 landing pads from top side of the ZX181V-HSPC.
Below is cross matrix outline of the signals in reference to row and column matrix.

Vita 57.4 HSPC signal access matrix



ZX181V-HSPC – Bottom view



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